ENW89811x4CF

Bluetooth QD ID: Published after Qualification

PAN1321-SPP

Infineon's
BlueMoonUniversal Platform

Wireless Modules

Panasonic
ideas for life

Edition 2008-07-07

Published by Panasonic Electronic Devices Europe GmbH,
Zeppelinstrasse 19,
D-21337 Lüneburg, Germany

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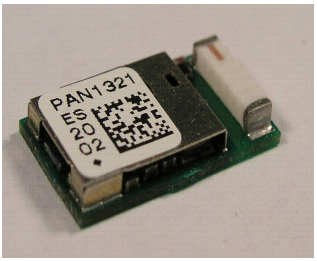
ENW89811x4CF

Revision History:	**2008-07-07**	DS-1321-2400-103-V0.9
Previous Revision:	First revision	

Section	Subjects (major changes since last revision)

1 General Device Overview



1.1 Features

General

- Complete Bluetooth 1.2, 2.0 and 2.0 + EDR solution
- Integrated stack with RFCOMM and SPP device profile
- Ultra low power design in 0.13 µm CMOS
- Temperature range from -40°C to +70°C (Optional +85°C)
- Integrates ARM7TDMI, RAM and patchable ROM
- On-module voltage regulators. External supply 2.9-4.1 V
- On-module EEPROM with configureable data
- Reference clock included
- Low power clock from internal oscillator or external low power clock (e.g. 32.768 kHz)
- Dynamic low power mode switching with request signal for clock and power supply

Embedded application

- Embedded application loaded from external EEPROM running on top of the integrated stack
- Easy development of customer specific embedded applications
- Standard application SW offered, for example SPP with AT commands over UART.

Interfaces

- 3.25 MBaud UART
- General purpose I/Os with interrupt and wake-up capabilities
- JTAG for boundary scan and debug

RF

- Transmit power programmable from -45 dBm to 4.5 dBm
- Transmit power typ. 2.5 dBm (default setings)
- Receiver sensitivity typ. -86 dBm at 2Mbit/s (DQPSK)
- Integrated antenna switch, balun and antenna filter
- Integrated LNA with excellent blocking and intermodulation performance
- No external components, integrated antenna
- Digital demodulation for optimum sensitivity and co-/adjacent channel performance

Bluetooth

- Scatternet with one slave role while still being visible
- Power control and RSSI
- Sniff mode
- Adaptive Frequency Hopping
- Quality of Service
- Bluetooth security features: Authentication, Pairing and Encryption
- Bluetooth test mode and Infineon's active Bluetooth tester mode and RF test modes

1.2 Ordering Information

Table 1-1 Ordering part number table

Ordering part number	Description	MOQ[1)]
ENW8Z811J4CF[2)]	Engineering Sample PAN1321 with SPP and max. +70°C (Consumer Range)	1
ENW8Z811K4CF[2)]	Engineering Sample PAN1321 with SPP and max. +85°C (Industrial Range)	1

1) Abbreviation for Minimum Order Quantity (MOQ)
2) As long as the module has engineering status, the sign ES are available on the label. The "Z" in the ordering part number indicates the engineering sample status. After mass production the "Z" will be changed to the "9" and the ES sign on the label will be deleted.

1.3 Block Diagram

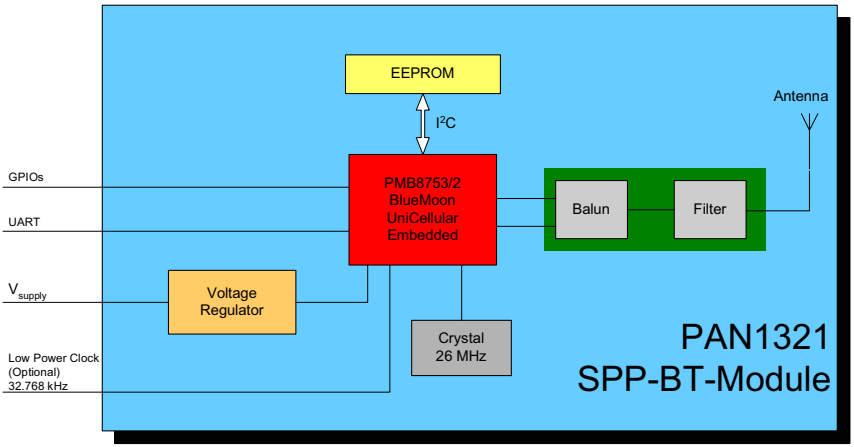


Figure 1-1 Simplified block diagram of PAN1321.

1.4 Pin Configuration LGA

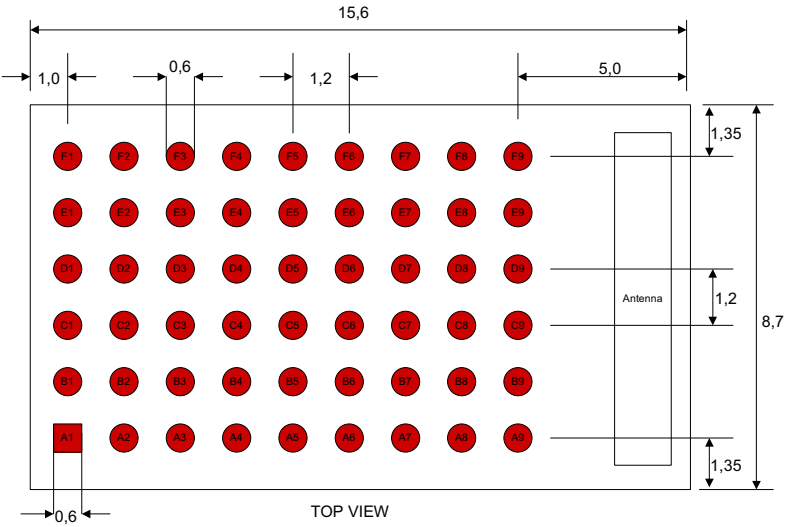


Figure 1-2 Pin Configuration for PAN1321 in Top View (footprint)

1.5 Pin Description

The non-shaded cells indicate pins that will be fixed for the product lifetime. Shaded cells indicate that the pin might be removed/changed in future variants. All pins not listed below shall be not connected.

Table 1-2 . Pin description table

Pin No.	Symbol	Pin Type	Supply voltage	During Reset	Function
A2	P1.6/ GATE_OUT	DIO-UD	Internal1	Z	Port 1.6 or Logic gate output
A3	RESET#	AI	Internal1	Input	Hardware Reset

Pin No.	Symbol	Pin Type	Supply voltage	During Reset	Function
A8	P1.5/ CLK32	DIO-UD	Internal1	Input	Port 1.5 or LPM clock input (e.g. 32.768kHz)
B1	P1.7	DIO-UD	Internal1	PD/ Input	Port 1.7
B2	P1.8	DIO-UD	Internal1	PD	Port 1.8
B3	P1.0/ TMS	DIO-UD	Internal2	PU[1)]	Port 1.0 or JTAG interface
B4	P1.4/ RTCK	DIO-UD	Internal2	Z	Port 1.4 or JTAG interface
B5	ONOFF	DI		-	Turns off module completely
B9	P0.15/ SLEEPX/ TST3	DIO-UD	VDDUART	PD	Port 0.15 or CLKIN & VDDSUP request or Test output
C2	P0.9	DIO-UD	Internal2	Z	Port 0.9
C3	JTAG#	DI	Internal2	PU	Mode selection Port 1: 0: JTAG 1: Port
C4	TRST#	DI	Internal2	PD	JTAG interface
D1	P0.10/ TST1	DIO-UD	Internal2	Z	Port 0.10 or Test output
D2	P0.8/ TST0	DIO-UD	Internal2	PD	Port 0.8 or Test output
D3	P1.1/ TCK	DIO-UD	Internal2	PU[1)]	Port 1.1 or JTAG interface
D4	P0.3	DIO-UD	VDD1	Conf. PD def.	Port 0.3
D5	P0.2	DIO-UD	VDD1	Z	Port 0.2
E1	P0.12/ SDA0	DIO-U	Internal2	PU	Port 0.12 or I2C data signal
E2	P0.13/ SCL0	DIO-U	Internal2	PU	Port 0.13 or I2C clock signal
E3	P1.3/ TDO	DIO-UD	Internal2	Z	Port 1.3 or JTAG interface
E4	P0.0	DIO-UD	VDD1	PD	Port 0.0
E5	P0.1	DIO-UD	VDD1	PD	Port 0.1
E6	P0.5/ UARTRXD	DIO-UD	VDDUART	Z	Port 0.5 or UART receive data
F2	P1.2/ TDI	DIO-UD	Internal2	PU[1)]	Port 1.2 or JTAG interface
F3	P0.11/ TST2	DIO-UD	Internal2	Z	Port 0.11 or Test output
F4	P0.14	DIO	VDDUART	Z	Port 0.14

Pin No.	Symbol	Pin Type	Supply voltage	During Reset	Function
F5	P0.7/ UARTCTS	DIO-UD	VDDUART	Z	Port 0.7 or UART CTS flow control
F7	P0.4/ UARTTXD	DIO-UD	VDDUART	PU	Port 0.4 or UART transmit data
F8	P0.6/ UARTRTS	DIO-UD	VDDUART	PU	Port 0.6 or UART RTS flow control
A4, A5, A6	VSUPPLY	SI		-	Power supply
C1	VREG	SO		-	Regulated Power supply
F6	VDDUART	SI		-	UART interface Power supply
C5	VDD1	SI		-	Supply voltage interface pads
A1, A7, A9, C8, C9, D7, D8, E8, E9, F1, F9	VSS			-	Ground

[1] Fixed pull-up/pull-down if JTAG interface is selected, not affected by any chip reset. If JTAG interface is not selected the port is tristate.

Descriptions of acronyms used in the pin list:

Acronym	Description
I	Input
O	Output
DI	Digital input
DIO-UD	Digital input/output with support for open drain, pull-up and pull-down
DIO-U	Digital input/output with support for open drain and pull-up
Z	Tristate
PU	Pull-up
PD	Pull-down
A	Analog (e.g. AI means analog input)
S	Supply (e.g. SO means supply output)

1.6 FW version

PAN1321 is available in different versions. Please check corresponding release documents for latest information.

1.7 System Integration

PAN1321 is a complete Bluetooth subsystem optimized for data transfer applications. It has all required interfaces and is designed to have a low bill of material (BOM) and small PCB area. The device includes Bluetooth protocol stack, HID and RFCOMM profiles in ROM. Additional profiles and application software can be downloaded to the system. **Figure 1-3** shows a typical SPP application.

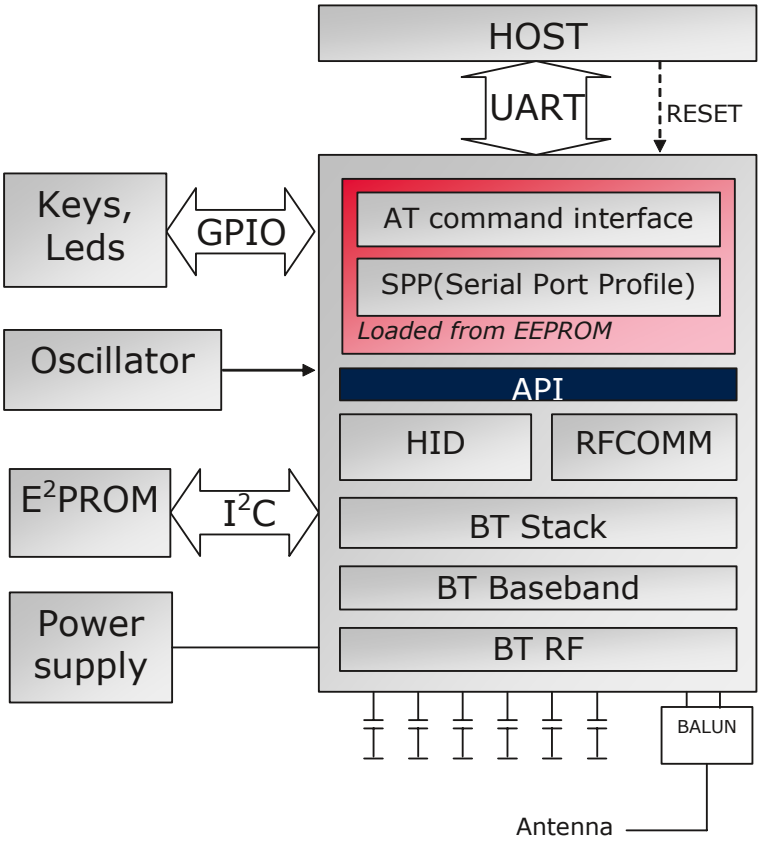


Figure 1-3 Example SPP application with PAN1321

Different interface options are available depending on the used profile and application. In all applications, the I2C interface is used for connection to the integrated EEPROM in PAN1321.

The EEPROM contain application software, additional profiles if needed and configuration data including the Bluetooth address.

Depending on application, the UART can be used for sending commands to PAN1321 and for transferring data to remote device. The 4-wire UART has an own power supply to ensure compatibility with the I/O voltages used by the system host.

Low power mode control of PAN1321 is implemented using signalling over the UART interface. Wake-up functionality of GPIOs can also be used to control low power modes. The host can reset PAN1321 via the RESET# signal, this methods will force PAN1321 to enter its lowest power mode. When using the ONOFF pin, the module will be turn off completely.

GPIOs are available in several voltage domains, programmable to be inputs or outputs and to have pull-up, pull-down or tri-state status.

PAN1321 supports clocking both from a crystal and from an existing reference clock. The low power clock (32 kHz) is generated internally, but an external 32 kHz clock can also be applied.

One single power supply is used to supply PAN1321. Integrated regulators supply all required voltages in the device.

The SLEEPX signal indicates when CLKIN and VSUPPLY are needed by PAN1321. This can be used to switch off the external oscillator and regulators when they are not needed.

2 Basic Operating Information

2.1 Power Supply

PAN1321 is supplied from a single supply voltage VSUPPLY (Pin A4, A5 and A6). This supply voltage must always be present. The Bluemoon UniCellular chip is supplied from an internally generated 2.5 V supply voltage. This voltage can be accessed from the VREG (Pin C1). This voltage may not be used for supplying other components in the host system but can be used for referencing the host interfaces.

The PCM interface and the UART interface are supplied with dedicated, independent, reference levels via the VDD1 (Pin C5) and VDDUART (Pin F6) pins. All other digital I/O pins are supplied internally by either 2.5 V (Internal2) or 1.5 V (Internal1). **Section 1.5** provides a mapping between pins and supply voltages.

The I/O power domains (VDD1 and VDDUART) are completely separated from the other power domains and can stay present also in low power modes.

2.2 Clocking

BlueMoon UniCellular has one clock input CLK32 that is optional. If used this 32.768 kHz clock must always be present to assist BlueMoon UniCellular to keep the time in low power modes.

The low power clock can be generated internally by the crystal oscillator and/or the low power oscillator or provided externally

2.3 Reset

There are differerent ways to reset PAN1321 with slightly different behavior. **Table 2-1** shows what happens to BD_DATA and patches for different types of reset.

Table 2-1 Different types of reset

	BD_DATA	Patches
Power-on reset	Set to default values	Disabled
External reset (RESET#)	Set to default values if *Save_RAM_BD_Data* = 0. Kept if *Save_RAM_BD_Data* = 1.	Disabled
HCI Reset issued by embedded application	Kept	Kept
Leaving manufacturer mode with Reset = 0x01	Kept	Disabled
Leaving manufacturer mode with Reset = 0x02	Kept	Enabled

2.4 Low Power Modes

To minimize current consumption, BlueMoon UniCellular automatically switches between different low power modes. The major modes are described below.

2.4.1 Clock Disabling Mode

As soon as a part of BlueMoon UniCellular is inactive, the clocks to that part are disabled. This can be done very quickly and is done without host intervention.

2.4.2 Low Power Mode

In Low Power Mode (LPM) most parts of BlueMoon UniCellular are powered down. The reference clock is still running. Entering and leaving LPM cannot be done as quickly as disabling/enabling clocks since internal state must be saved and restored, but the power consumption is lower in LPM. The minimum time of inactivity that is required to enter LPM is configured with the BD_DATA parameter *LPM_Threshold*.

In addition to this dynamic control, low power modes must be globally enabled. This is done by the embedded application or with an AT command in the SPP application case. The value *Default_LPM_Mode* in BD_DATA parameter *LPM_Conf* controls if low power modes are enabled or disabled after reset. The value *AutoDisable_LPM* in the same parameter controls if low power modes should be disabled after host initiated wakeup.

2.4.3 Ultra Low Power Mode

Ultra Low Power Mode (ULPM) is similar to LPM with the addition that the reference clock may be switched off. If VDDPM is externally supplied, the main supply voltage VDDSUP may also be switched off. Bluetooth state is updated using the low power clock. Leaving ULPM takes longer time than leaving LPM because the reference clock must be started. The minimum time of inactivity that is required to enter ULPM is configured with the BD_DATA parameter *ULPM_Threshold*. The accuracy of the low power clock is specified with the parameter *LPM_Drift*.

The signal SLEEPX is used to indicate when BlueMoon UniCellular enters ULPM. **Figure 2-1** shows an example with the default polarity of SLEEPX. When SLEEPX goes low the system is allowed to switch off VDDSUP and CLKIN. When BlueMoon UniCellular wants to leave ULPM it sets SLEEPX high again to request VDDSUP and CLKIN. The internal low power state machine waits for a time *Osc_Settle* for the power supply and clock to stabilize before starting the rest of the system. The parameter *Osc_Settle* is configurable in BD_DATA.

ULPM is controlled and enabled in the same way as LPM.

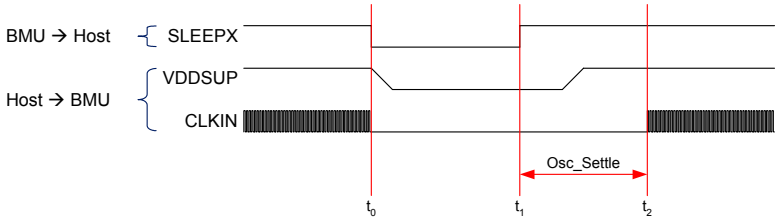


Figure 2-1 SLEEPX indicating Ultra Low Power Mode

2.4.4 Complete Power Down

If Bluetooth functionality is not needed at all, VDDSUP and VDDPM should be grounded to minimize power consumption. In this state there is no activity in BlueMoon UniCellular and the Bluetooth state (native clock, etc.) is not updated.

2.5 SLEEPX Configurations

The SLEEPX signal can be configured in different ways to fit the host system's clock and power supply requests. The behavior after firmware startup can be configured with HCI+ commands and BD_DATA parameters. The polarity of SLEEPX can be selected with a bit in the BD_DATA parameter *BB_Conf*. Some typical system configurations are shown below.

Separate Power Supply and Clock Request Signals

The simplest case is when BlueMoon UniCellular and the rest of the system has separate signals to request power and clocks. This is shown in **Figure 2-2**.

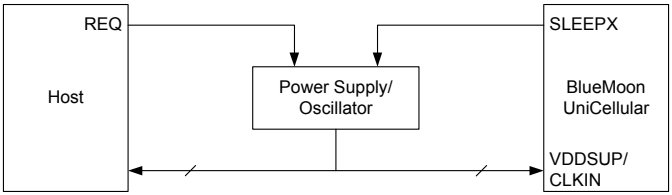


Figure 2-2 Separate Power Supply and Clock Request Signals

Shared Power Supply and Clock Request Signals

If the SLEEPX signal and the host's request signal are configured to pull in one direction and drive in the other, it is possible to wire the signals together. This is shown in Figure 2-3.

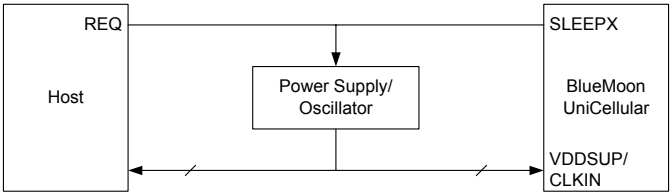


Figure 2-3 Shared Power Supply and Clock Request Signals

3 Interfaces

3.1 UART Interface

The UART interface is the main communication interface between the host and PAN1321 in applications where serial port communication is included. One example is the SPP application, where communication is made with AT commands over the UART.

In the case of a customer specific embedded application, the UART can be controlled by the application through an API described **Ref [1]**.

The interface consists of four UART signals as shown in **Figure 3-1**. Depending on the application, some or all of the signals are needed.

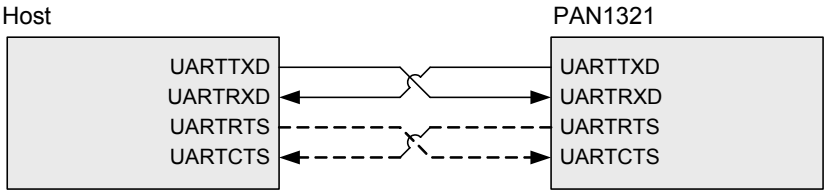


Figure 3-1 UART Interface

3.1.1 UART

The on-chip UART (Universal Asynchronous Receiver and Transmitter) is compatible with standard UARTs. Hardware support for SLIP[1)] framing and 16-bit CRC calculation is available for embedded applications. A separate supply voltage, VDDUART, makes it easy to connect the UART interface to any system.

3.1.1.1 Baud Rates

The UART baud rate can be configured by the application through the API described in **Ref [1]**.

The supported baud rates are listed in **Table 3-1** together with the small deviation error that results from the internal clock generation. The default baud rate is 115200 Baud.

1) See http://www.ietf.org/rfc/rfc1055.txt for information about SLIP.

Table 3-1 UART Baud Rates

Wanted Baud Rate	Real Baud Rate	Deviation Error (%)
9600	9615	0.16
19200	19230	0.16
38400	38461	0.16
57600	57522	-0.14
115200	115044	-0.14
230400	230088	-0.14
460800	464285	0.76
921600	928571	0.76
1843200	1857142	0.76
3250000	3250000	0

3.1.1.2 Detailed UART Behavior

After reset the UART interface is configured with one start bit, eight data bits, no parity bit and one stop bit. The least significant bit is transmitted first.

The polarity of the UART signals can be changed by the application software through the API described in **Ref [1]**. The default (non-inverted) behavior is shown in **Table 3-2**

Table 3-2 Default (non-inverted) behavior of UART signals

Signal	Level	Meaning
UARTTXD / UARTRXD	0	Start bit, ’0’ bit in character.
	1	Idle level, stop bit
UARTRTS / UARTCTS	0	Flow on
	1	Flow stopped

To prevent the system from floating signal lines while PAN1321 is in low power mode, the application software can activate internal pull-up or pull-down resistors through the API described in **Ref [1]**.

UARTCTS Response Time

Figure 3-2 shows the UARTCTS response time. Assuming non-inverted UART signals, the data flow stops within the “flow off response time” after UARTCTS has been set to high. If UARTCTS goes high during the transmission of a byte (phase 1 in the figure) this

byte will be completely transmitted. While UARTCTS is high, no data will be transmitted (phase 2). When UARTCTS goes low again, data transmission will continue (phase 3).

The maximum flow off response time is 10 UART bits (including start and stop bits). As an example, if the UART baud rate is 115200 Baud, the maximum flow off response time is 10 x 1/115200 s = 87 µs.

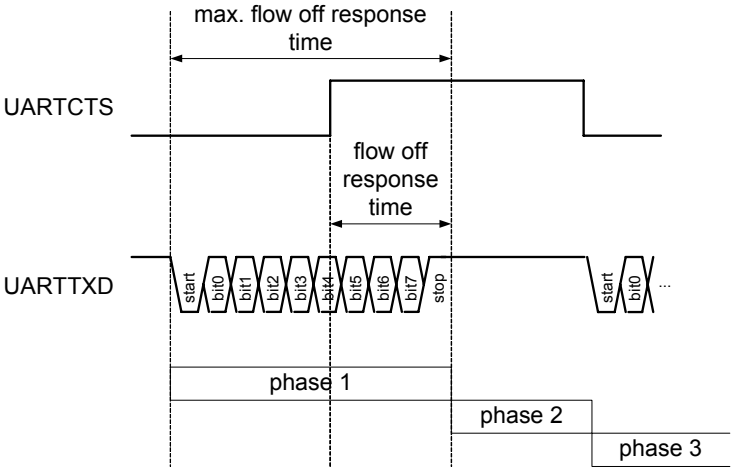


Figure 3-2 UARTCTS response time

3.1.2 Low Power Mode Protocol

In PAN1321 the general Low Power Mode settings are governed by the BD_DATA .

The real-time handling of Low Power Modes are handled by the application software through the API described in **Ref [1]**.

For standard applications using the UART, like the SPP application, the behaviour is described in the corresponding Software Description Document.

3.2 GPIO Interface

3.2.1 General Purpose I/Os

Most digital pins on PAN1321 can be used as general purpose I/Os (GPIOs). The GPIO pins are grouped into two ports: P0 and P1. P0 has 16 pins (P0.0 - P0.15) and P1 has nine pins (P1.0 - P1.8). Information about each pin's placement and capabilities can be found in the pin description in **Section 1.5**.

The GPIOs are completely controled by the application software through the API (described in **Ref [1]**). For standard applications the control of GPIOs is described in the corresponding Software Description documents.

3.3 Internal EEPROM / I2C Interface

PAN1321 supports storage of non-volatile information in the internal EEPROM connected to the I2C interface.

The EEPROM contains the following partitions:

- The Bluetooth Device Data (BD_DATA) Storage
- The Application and patches to the firmware
- Application data (any application specific data)
- Production default values

The partition table and each partition are protected by checksums.

The partition table and the partions in EEPROM are described in detail in **Ref [1]**.

The application software can read and write to the EEPROM through the API described in **Ref [1]**, through standard HCI commands (e.g. HCI_Change local name) or through Infineon specific HCI+ commands (e.g. Infineon_write_BD_Data).

3.3.1 I2C Hardware

The I2C hardware is compatible with standard I2C interfaces. It supports data rates of up to 400 kbit/s. Currently only 7-bit addressing and master mode is supported.

The application software can access the I2C Hardware through the API described in **Ref [1]**.

4 General Device Capabilities

This chapter describes features available in the PAN1321 core.

Actual feature set and how to access the features can be found in **Ref [1]** in case of access from an embedded customer application or in the corresponding Software Description Documents for standard applications.

4.1 Embedded Application

At startup or reset, PAN1321 loads the embedded application from external EEPROM into internal RAM and starts the application. If no valid application is found in the EEPROM, PAN1321 starts a default ROM application. This application will restart the chip to retry loading the application.

Thus, to work correctly, PAN1321 requires an external EEPROM that has been programmed with an external programming tool.

In the case of a Standard Application from Infineon, e.g. the SPP application, Infineon supplies a complete EEPROM image.

In the case of a customer specific application, the user can write the application in C or assembly language and produce the EEPROM image through a tool-chain consisting of Infineon supplied tools and commercially available SW development tools.

During development of a customer specific embedded application, it is also possible to load the application directly into the internal RAM with a JTAG debugger.

How to produce a customer specific EEPROM image and how to load and debug an embedded application is described in detail in **Ref [1]**.

4.2 HCI+ and Bluetooth Device Data (BD_DATA)

In addition to the standard Bluetooth HCI commands and events, PAN1321 supports a set of Infineon specific commands and events called HCI+. All Infineon specific features are accessed using the HCI+ commands described in **Ref [1]**.

All configuration information that is critical for correct operation of PAN1321 is called Bluetooth Device Data (BD_DATA). This data is stored in PAN1321's internal RAM for fast access and in non-volatile memory (external EEPROM).

4.3 Firmware ROM Patching

4.3.1 Patch Support

PAN1321 contains dedicated hardware that makes it possible to apply patches to any code and data in the firmware ROM. The hardware is capable of replacing up to 32 blocks of 16 bytes each with new content.

Figure 4-1 shows an example where two blocks in firmware ROM have been replaced. The dashed arrow shows that the second block makes use of code and/or data in the RAM area.

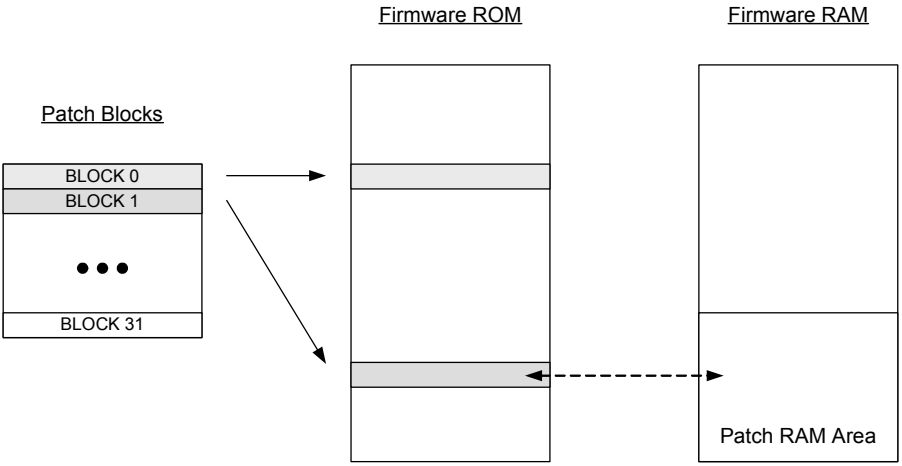


Figure 4-1 Patch Hardware

4.3.2 Handling Patches

In PAN1321 the patches are stored in a partition of the external EEPROM. At start up, the firmware copies the patch data to internal RAM and sets up the hardware to enable the patches.

If patches are needed in the Standard Application case, they are included in the EEPROM image containing all other EEPROM partitions (Standard Application, BD Data, etc.) and shall be programmed into the EEPROM using external tooling. This EEPROM image is supplied by Infineon.

For a customer specific application, the EEPROM image including any necessary patches is produced with tooling described in **Ref [1]**.

4.4 Hardware and Software Version Information

The application can get detailed information about the hardware and software versions of PAN1321 using HCI+ commands described in **Ref [1]**.

4.5 Advanced Error Reporting

PAN1321 has the capability to detect and report various error conditions to the application. The following types of errors can be distinguished:

Fatal Exception: A fatal error has been detected and PAN1321 cannot continue normal operation. The device performs a reset and reports the error with an Infineon Fatal Exception event.

Debug Exception: An error has been detected but PAN1321 can continue normal operation. The exception is reported with an Infineon Debug Exception event.

Hardware Error: Hardware error conditions are reported with the Hardware Error event that is defined in the Bluetooth specification.

Watchdog Reset: A watchdog timer guarantees that PAN1321 is restarted if the firmware stops working for some reason. The condition is reported with a Hardware Error event.

The reporting is done through HCI+ events to the application. The events and how to clear the exceptions are described in **Ref [1]**.

5 Bluetooth Capabilities

5.1 Supported Features

PAN1321 supports all mandatory and optional features in the Bluetooth 2.0 + EDR specification, except for the features listed in **Chapter 5.2**.

Including:

- Enhanced Data Rate up to 3 Mbit/s
- Adaptive Frequency Hopping (AFH)
- All ACL packet types
- All LMP features
- Authentication, Pairing and Encryption
- Quality of Service
- Sniff
- Role Switch
- RSSI and Power Control
- Power class 2 and 3
- Scatternet with one slave role while still being visible
- Standard Bluetooth test mode, Active Tester Mode and RF Test Modes

5.2 Not Supported features

- Synchronous links
- Hold mode
- Park state
- Broadcast
- CQDDR
- HCI remote loopback

5.3 PAN1321 Specifics and Extensions

This chapter describes features available in the PAN1321 core.

Actual feature set and how to access the features can be found in:

- **Ref [1]** in case of access from an embedded application
- the corresponding Software description Document in case of a standard application

5.3.1 Configurable LMP Features

PAN1321 supports all feature bits that are defined in the Bluetooth 2.0 + EDR specification. The host can disable unwanted LMP features with the BD_DATA parameter *LMP_Features*. The following rules apply:

- A feature is fully supported if the corresponding feature bit is set.

- If a feature bit is not set, the link manager behaves as if the feature was not supported. If the feature is requested by the local host or the remote link manager the request will be denied.
- Depending on the feature bits, PAN1321 behaves as a Bluetooth 1.1, 1.2 or 2.0+EDR device. If at least one of the feature bits corresponding to Bluetooth 1.2 (e.g. AFH) is set, PAN1321 behaves as a Bluetooth 1.2 device. If at least one of the feature bits corresponding to Bluetooth 2.0+EDR (e.g. 3-slot EDR packets) is set, PAN1321 behaves as a Bluetooth 2.0+EDR device.

Some of the feature bits do not follow the general rules:

- **Flow Control Lag:** The flow control lag is a characteristic of the firmware and cannot be configured. The *Flow Control Lag* bits should be set to zero.
- **Enhanced Inquiry Scan:** Enhanced Inquiry Scan is always used whether or not the feature bit is set.

A list of all features can be found in section 3.3 in the Bluetooth 2.0 + EDR specification.

5.3.2 Local Device

5.3.2.1 HCI Command Flow Control

PAN1321 is able to buffer two HCI command packets and starts performing the commands in the order in which they are received. Execution of a command can be started before the previous command has been completed. Commands that involve the page procedure (i.e. HCI_Create_Connection and HCI_Remote_Name_Request) cannot be performed at the same time since two page procedures cannot be performed simultaneously; the second command will be delayed until the first has completed.

5.3.2.2 HCI Buffers

PAN1321 supports the following number of HCI buffers and buffer sizes (as returned by the HCI_Read_Buffer_Size command):

Table 5-1

Type	Number of Buffers	Size of each Buffer
ACL	11	339

5.3.2.3 Event Filtering

Up to 15 event filters are supported with the HCI command Set_Event_Filter.

5.3.2.4 Local Name

PAN1321 can store a local name with a length of 100 bytes (excluding the 0x00 termination character). The local name can be stored in RAM or in non-volatile memory (external EEPROM). The place of storage is configured with the *Local_Name* field in the BD_DATA parameter *BB_Conf*.

5.3.3 Discovery and Connection Establishment

5.3.3.1 Multiple Inquiry Access Codes

PAN1321 can scan for up to five inquiry access codes (IACs) during inquiry scan. The number can be read with HCI_Read_Number_Of_Supported_IAC. The IACs can be read and written with HCI_Read_Current_IAC_LAP and HCI_Write_Current_IAC_LAP.

The IACs will be used cyclically in consecutive scan windows. The number of IACs has no influence on the scan window and scan interval settings. Consequently, the overall scan time for each IAC is proportionally reduced. If interlaced scan is enabled, the same IAC is used for both interlaced scan windows. The IACs provided by the host may be identical to allow prioritization of one IAC over the others.

Figure 5-1 shows the use of multiple IACs.

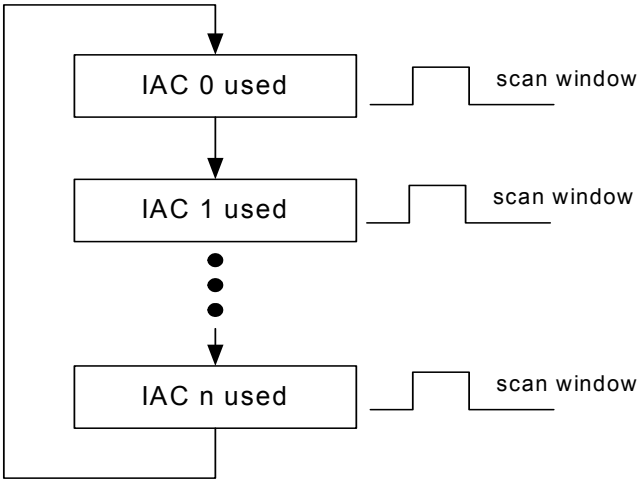


Figure 5-1 Use of Multiple IACs

5.3.3.2 Page and Page Scan

PAN1321 supports the mandatory paging scheme, paging modes P0, P1 and P2 and scan repetition modes R0, R1 and R2. The default page scan repetition mode is R1.

5.3.4 During Connection

5.3.4.1 Scatternet and Piconet Capabilities

PAN1321 supports point-to-point and scatternet scenarios:

- Up to 2 links
- Maximum 1 simultaneous slave role
- Always capable of responding to inquiry and remote name request
- Always capable of Inquiry

5.3.4.2 Role Switch

Only one role switch can be performed at a time. If a role switch request is pending, other role switch requests on the same or other links are rejected. If a role switch fails, PAN1321 will automatically try again a maximum of three times. Encryption (if present) is stopped in the old piconet before a role switch is performed and re-enabled when the role switch has succeeded or failed. If the physical link is in Sniff a role switch will not be performed.

5.3.4.3 Dynamic Polling Strategy

In addition to the regular polling scheme, PAN1321 dynamically assigns unused slots to links where data is exchanged. This adapts very well to bursty traffic and improves throughput and latency on the links.

5.3.4.4 Adaptive Frequency Hopping (AFH)

PAN1321 supports adaptive frequency hopping according to the Bluetooth 2.0 + EDR specification. AFH switch and channel classification are supported both as master and slave. Channel classification from the host is also supported.

A number of HCI+ commands and events are available to provide information about AFH operation. The commands Infineon_Enable_AFH_Info_Sending and Infineon_Disable_AFH_Info_Sending turn on and off the Infineon AFH Info events that provide detailed information about channel classification, channel maps, interferers, etc.

If enabled by the Infineon_Enable_Infineon_Events command, the Infineon AFH Extraordinary RSSI event informs the host whenever extraordinary RSSI measurements in unused slots have been started. This is done when the number of known good channels has decreased below a critical limit and periodically after a defined time.

The Infineon_Set_AFH_Measurement_Period command can be used to configure the duration of the AFH measurement period.

5.3.4.5 Quality of Service (QoS)

PAN1321 supports quality of service according to the Bluetooth 2.0 + EDR specification. It is recommended to use the HCI_Flow_Specification command to set the QoS parameters for both outgoing and incoming traffic. The old HCI_QoS_Setup command can be used to set the QoS parameters for outgoing traffic.

The outgoing QoS parameters Access_Latency/Latency and Token_Rate are used to set the poll interval. The incoming QoS parameter Access_Latency is used to define the maximum reassembly time. (To optimize throughput, PAN1321 tries to fill internal buffers before sending received data to the host. If a buffer has not been filled “maximum reassembly time” after a packet has been received, the buffer will be sent to the host anyway.) The default maximum reassembly time is the same as the default poll interval (40 slots).

If both QoS and EDR are enabled in PAN1321 and supported by the remote device, PAN1321 automatically tries to switch to EDR if the QoS bandwidth requirements are too high to be supported by basic rate. For power saving reasons, the QoS algorithm makes use of EDR packets whenever the RF quality is high enough.

In order to make the QoS algorithm work efficiently the host should always allow all packet types. It may disallow the use of 5-slot packets or restrict the packet types to 1-slot packets completely but should not use other combinations.

5.3.5 Security

5.3.5.1 Authentication

Authentication can be performed at connection creation or during connection.

The repeated attempts algorithm described in section 5.1 in the Bluetooth 2.0 + EDR specification is implemented with the following parameters:

The first waiting interval is 5 seconds. After each subsequent authentication failure the waiting interval is doubled. Every 30 seconds the waiting interval falls back one step. The maximum waiting interval is 40 seconds.

5.3.5.2 Link Key Management

Up to five link keys can be stored with HCI_Write_Stored_Link_Key. The link keys are stored in RAM or non-volatile memory if available.

5.3.5.3 Encryption

Encryption can be enabled at connection creation or during connection if an authentication has been performed. Both point-to-point and broadcast encryption are supported.

When PAN1321 is connected to several other devices as master and broadcast encryption is requested, a common encryption key length will be chosen to maximize the number of devices that can be included in the broadcast encryption group. Devices that cannot accept the settings will be disconnected.

The minimum and maximum encryption key sizes accepted by PAN1321 can be set and read with the HCI+ commands Infineon_Set_Encryption_Key_Size and Infineon_Read_Encryption_Key_Size.

5.3.5.4 Pairing

The HCI+ command Infineon_Write_Pairing_Mode can be used to set PAN1321 in pairable or non-pairable mode.

5.3.6 RSSI and Output Power Control

5.3.6.1 Received Signal Strength Indication (RSSI)

PAN1321 supports received signal strength measurements and uses LMP signaling to keep the output power of a remote device within the golden receive power range. The range is set with the BD_DATA parameters *RSSI_Min* and *RSSI_Max*.

5.3.6.2 Output Power Control

PAN1321 supports power control according to the Bluetooth 2.0 + EDR specification.

- The output power can be controlled in 3 or 4 steps (configurable). PAN1321 can work as a class 2 or 3 device depending on the settings.
- Fine tuning can be used on the power steps.

The following BD_DATA parameters are used for configuration:
RF_Psel_D, RF_Psel_Conf, RF_Conf, TX_Power_Ref#.

5.3.6.3 Ultra Low Transmit Power

For high security devices the output power can be reduced to a value that reduces the communication range to a few inches. This mode is enabled with the HCI+ command Infineon_TX_Power_Config.

5.3.7 Test Modes

PAN1321 supports the standard Bluetooth test mode (DUT) and two Infineon specific test modes, Active Tester Mode and RF Test Modes.

5.3.7.1 Active Tester Mode

PAN1321 can act as a Bluetooth RF tester running the Bluetooth test mode. All defined test mode scenarios can be configured and initiated with the HCI+ command Infineon_Active_Tester. Detailed information about the active tester mode is available in the HCI+ specification in **Ref [1]**.

5.3.7.2 RF Test Modes

RF transmitter and receiver measurements can be done in the following test modes:

- TX burst mode
- RX burst mode
- RX burst mode with data transparently sent to host
- RX bit & packet error rate measurement mode

The modes are configured with the HCI+ command Infineon_Test_Mode. Detailed information about the modes is available in the HCI+ specification in **Ref [1]**.

5.3.7.3 EDR Packet Test Command

The HCI+ command Infineon_Test_EDR_Packets can be used to force PAN1321 to use enhanced data rate or basic rate. This will be done without LMP negotiation and should only be used for testing.

5.3.8 Debugging

5.3.8.1 LMP Tracing and Sending

An LMP trace mode makes it possible to trace the LMP traffic between PAN1321 and other devices without an external protocol analyzer. The LMP PDUs that are sent and received are sent to the host with the Infineon LMP PDU Trace event. The trace events are activated with the Infineon_Activate_Deactivate_Traces command.

It is also possible to send an LMP PDU to another device. This is done with the HCI+ command Infineon_Send_LMP.

5.3.8.2 Error Events

The following Infineon specific error events exist:

Table 5-2 Error Event Table

Event	Description
Infineon Invalid ACL_BC_PB Flag	Indicates that PAN1321 has received an HCI packet with invalid BC or PB flag from the host.
Infineon Invalid ACL_CNC_Handle	Indicates that PAN1321 has received an ACL HCI packet with invalid connection handle from the host.

5.3.8.3 Information Events

With the HCI+ command Infineon_Enable_Infineon_Events it is possible to enable and disable the following information events:

Table 5-3 Information Event Table

Event	Description
Infineon PTT Switch Notification	Indicates that the packet type table (PTT) has been switched.
Infineon Scan Status	Indicates that the link manager has temporarily changed the scan settings provided by the host.
Infineon Debug Exception	Indicates an internal problem in PAN1321.

6 AT-Specification

6.1 Introduction

This chapter describes the AT commands applicable to Panasonic's PAN1321 Bluetooth solution for embedded applications. The product utilizes a raw AT set of commands and events over UART command set for Bluetooth communications and control on an embedded device.

Please refer to **Ref [3]** for actual status of the SPP software.

6.2 Serial Port Profile

Host communication sent over UART is always called command except while in stream mode, see below. All communication received by host application over UART is called response except while in stream mode.

6.2.1 Operation Modes

The specification defines two operation modes of the PAN1321-SPP. For Bluetooth SPP there are furthermore two different roles specified; A-device (paging device) setting up the over the air connection and B-device which is connectable and accepts the connection (page scanning device).

6.2.1.1 Command mode

In this mode the SPP application running on the PAN1321 will execute the AT commands sent from the Host over the UART using the H4 UART protocol as specified within the Bluetooth SIG [**Ref [2]**]. In this mode, the Host application can send data to the PAN1321, which are transmitted to the other device which has a Bluetooth connection on SPP level with the PAN1321. This mode is normally used when transmitting bursty and packetized data. Setting up/accepting Bluetooth SPP connections and/or searching for other Bluetooth devices are also other operations done in this mode.

6.2.1.2 Stream mode

In this mode, the Host application will send un-packatized data to the PAN1321, and is transmitted over the air to the other device. This mode is normally used when transmitting small size of data in a random way and for serial cable replacement applications.

6.2.2 Pin Assignments

Table 6-1

Pin Name	Module Pin Number	IC Pin Number	Direction	Description
UART_RXD	E6	P0.5 (Reserved)	I	UART
UART_TXD	F7	P0.4 (Reserved)	O	UART
UART_RTS	F8	P0.6 (Reserved)	O	UART
UART_CTS	F5	P0.7 (Reserved)	I	UART
SDA	E1	P0.12 (Reserved)	I	I2C
SCL	E2	P0.13 (Reserved)	I	I2C
GPIO 0	E4	P0.0	I/O	LPM
GPIO 8	F4	P0.14	I/O	LPM
GPIO 1	E5	P0.1	I/O	APPL GPIO
GPIO 2	D5	P0.2	I/O	APPL GPIO
GPIO 3	D4	P0.3	I/O	APPL GPIO
GPIO 4	D2	P0.8	I/O	APPL GPIO
GPIO 5	C2	P0.9	I/O	APPL GPIO
GPIO 6	D1	P0.10	I/O	APPL GPIO
GPIO 7	F3	P0.11	I/O	APPL GPIO
GPIO 9	B9	P0.15	I/O	APPL GPIO

6.3 AT SPP command and response

AT commands can only be sent while in command mode with the exception of stream connection cancel (^^^) which can be sent in stream mode. The expected response after sending an AT command is the "OK" response, see specification below. The host shall wait for a command to be terminated before sending a new one. A command is considered as terminated when "OK" and all subsequent related responses have been received.

There are also reponses, which are not initiated by a sent command. They are in that case initiated by the remote Bluetooth device.

6.3.1 AT command and response format and syntax

All data exchanged between the host and eBMU is in ASCII format.

Parameters for commands and responses are given in decimal (DEC) base in ASCII format unless hexadecimal (HEX) base is specified.

MSB is always sent first. eBMU does not distinguish between upper and lower cases.

Example for values with decimal base in ASCII format:

The number 255 in decimal corresponds to the following three characters ‘2’, ‘5’, ‘5’. E.g. AT+JSDA=010,1234567890 (the number 10 is given by three ASCII characters ‘0’, ‘1’, ‘0’.

Example for values with hexadecimal base in ASCII format:

The number 255 in decimal base corresponds to the number FF in hexadecimal base, thereby the number in ASCII format for hexadecimal base is represented by the following two characters ‘F’, ‘F’.

E.g. +RSNFCNF=3E80,2 ; The four ASCII characters ‘3’, ‘E’, ‘8’, ‘0’ represent the number 3E80 in hexadecimal base which corresponds to 16000 in decimal base.

6.3.1.1 AT-commands

All AT-commands follow the format below:

AT+<command>=<parameter 1 (if required)>,<parameter 2 (if required)>,<parameter 3 (if required)> ,<…><carriage return><line feed>

E.g.: AT+JCCR=0010c64d67dc,01 (to connect to BD_ADDR "0010c64d67dc", service channel 1)

6.3.1.2 AT-responses

All AT-responses follow the format below with the exception of <OK> and <ERROR=>;

+<response>=<parameter 1 (if required)>,<parameter 2 (if required)>,<parameter 3 (if required)>,<…><carriage return><line feed>

E.g.: +RDAI =0010c64d67dc,DATA ("DATA" received from 0010c64d67dc)

6.3.1.3 AT response parameter list for <status>, <state> and <ERROR>

- Values for <status> general for all commands

Table 6-2 Command execution status value table

Values for <status> general for all commands	Status Value
BT_OK	0
BT_CONGESTED	1
BT_CALL_ERROR	2
BT_CONTROL_CMD_COMPLETE	3
BT_CONTROL_CMD_PENDING	4
BT_FAILED	5
BT_BAD_CONFIG	6
For future use	7-15

- General error messages.

Table 6-3 General Error Message Table

Error Message	Error Code
SPP Error	0
Syntax Error	-1
Command not allowed at present general status	-2

6.3.2 AT command list table

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JAAC= <auto_accept>	**Auto Accept Connection requests** Forces PAN1321 to accept connection requests. auto_accept parameter (1 octet): 0 - Host will be notified on incoming connection indication (+RCOI) - (no auto accept). Default value 1 - PAN1321 will automatically auto accept incoming connection request - (host will be notified but connection is accepted automatically)	OK	Dev B
AT+JACR= <accept>	**Accept Connection Request** Shall be used as answer to a connect indication (+RCOI). accept parameter (1 octet): 0 - Not accepted 1 - Accepted	OK	Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JEDT	**Enable Device under Test** This SPP-AT command enables the device under test. After this command has been sent it is possible for a remote tester to connect, this AT command corresponds to the three different HCI commands listed below: 1. Set Event Filter - allow all connections. 2. Write Scan Enable - page and Inquiry. 3. Enable device under test. Note: JEDT command can only be issued with security mode 1 and after production mode is enabled (JPRO=1).	OK	Dev A Dev B
AT+JCAC= <trim_value>,<GPIO >	**Crystal Auto Calibrate** trim_value parameter (4 octets / HEX base): The trim value is used to adjust the frequency on the GPIO chosen by the GPIO parameter. GPIO parameter (4 octets / HEX base): Two GPIOs can be used as output for the 32768 Hz clock P01 and P08 (0002 and 0100). Note: JCAC command can only be issued after production mode is enabled (JPRO=1).	+RCACCNF= <osc_trim> osc_trim parameter(4 octets / HEX base) Use AT+JCBD to store the osc_trim value to EEPROM.	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B

AT+JCBD=<bd_data>	**Change BD_Data**
	bd_data parameter (116 octets / HEX base): (reference values)
	msg.bdAddr (12 octets)= see note1
	msg.channelWordOffset (4 octets) =0000;
	msg.clkConf (2 octets)= 8A;
	msg.eepromSize (2 octets)=80;
	msg.inputFreq (8 octets)=018CBA80;
	msg.lmpFeatures (16 octets)=000019987E0602BF;
	msg.lpmConf (2 octets)=40;
	msg.lpmDrift (2 octets)=FA;
	msg.lpmThreshold (2 octets)=12;
	msg.ulpmThreshold (2 octets)=18;
	msg.pmuConfig (4 octets)=0080;
	msg.rfPselD (8 octets)=06050403;
	msg.rfPselConf (2 octets)=44;
	msg.rssiMin (2 octets)=0C;
	msg.rssiMax (2 octets)=10;
	msg.ddcTlConf (2 octets)=02;
	msg.uartBaudrate (2 octets)=04;
	msg.uartInvert (2 octets)=00;
	msg.uartPulls (2 octets)=01;
	msg.oscSettle (2 octets)=08;
	msg.bbConf (2 octets)=04;
	msg.rfConf (2 octets)=04;
	msg.txPowerRef0 (2 octets)=F2;
	msg.txPowerRef1 (2 octets)=F8;
	msg.txPowerRef2 (2 octets)=FE;
	msg.txPowerRef3 (2 octets)=04;
	msg.oscTrim (4 octets)=see note 2;
	msg.threeWireArqTimeout (2 octets)=06;
	msg.LMP_Version (2 octets)=00;
	msg.Reserved (16 octets)=0000000000000000;
	
	Note 1: This value shall be configured with the desired Bluetooth device Address (e.g. FFAA010203BB).
	
	Note 2: This value shall be configured with the value found during crystal calibration (see command AT+JCAC).
	
	Note 3: JCBD command can only be issued after production mode is enabled (JPRO=1). Changes in BD Data take place after production mode command is disabled (JPRO=0) followed by a SW reset (AT+JRES).
		OK	Dev A
			Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JCCR=<bd_addr>, <service channel>	**Create Connection Request** Instructs PAN1321 to connect to a remote Bluetooth device (prospective slave). bd_addr parameter (12 octets / HEX base): The Bluetooth address of the remote device service_channel parameter (2 octets / DEC base): 0-30 Which service channel to connect to can be received from a Service Discovery (AT+JSDS)	OK (Followed by): +RCCRCNF=<MTU_ size>,<status> MTU_size parameter (3 octets / DEC base) status parameter (1 octet) If maximum number of allowed connections already exists: ERR=0.	Dev A
AT+JDDS= <limit_inquiry_result>	**Device Discovery Start** Causes PAN1321 to start a Device Discovery (Inquiry and Remote Name Request) of the Bluetooth neighborhood. limit_inquiry_result parameter (1 octet): 0- The maximum number of responses that can be obtained is 8. 1- The number of responses will be 8 devices.	OK (Then, if responses are returned): +RDDSRES= < bd_addr > <remote_name>, <COD> (For each response) bd_addr parameter (12 octets / HEX base). remote_name parameter (variable length): Name of the remote device. Page Timeout is received as a name if the remote name is not found during device discovery COD parameter (6 octets / HEX base). Class of device (Completed by): +RDDSCNF=<status> status parameter (1 octet)	Dev A

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JDIS= <discoverable>	**DIScoverable** Forces PAN1321 into Page Scan / Inquiry Scan states indefinitely (note: this makes the device discoverable). discoverable parameter (1 octet): 0-No scans enabled. 1-Inquiry Scan enabled. 2-Page Scan enabled. 3-Inquiry & Page Scan enabled. Note: Default value after a HW reset is no scans enabled	OK	Dev B Dev A can be discoverable but not accept incoming connections.
AT+JDOI	**DOwnload Application Image via UART** After "OK" response a binary file with the EEPROM image should be sent. File open and send in binary format after "OK" is received. Note: JDOI command can only be issued after production mode is enabled (JPRO=1). Changes in the EEPROM image are effective after production mode command is disabled (JPRO=0) followed by a HW reset.	OK after command is sent. +RDOICNF after .eep file has been written. Note: PAN1321 calculates the size of the image that is being downloaded from the file header. The response +RDOICNF is generated when the calculated size is reached.	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JGPA=<read>, <set>,<clear>	**GPIO action** All parameters of this command are bit fields of 16 bits corresponding to GPIOs P0.15 to P0.0. E.g. if pin P0.0 is the desired bit; the bit field value is 0001 and if the desired bit is P0.12 the bit field value is 0800. read parameter (4 octets / Hex base): Values for each bit: 0- No Action 1- Read set parameter (4 octets / HEX base): Values for each bit: 0-No Action 1-Set clear parameter (4 octets / HEX base): Values for each bit: 0-No Action 1- Clear	+GPOACNF=<value> value parameter (4 octets / HEX base): This value is the state of the GPIO PINs specified in read parameter. Values for each bit: 0 - means low. 1 - means high.	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JGPC= <direction>, <open_drain>, <pull_on/off>, <pull_up/down>, <tristate>	**GPIO Configuration** All parameters of this command are bit fields of 16 bits corresponding to GPIOs P0.15 to P0.0 (See command AT+JGPA). direction parameter (4 octets / HEX base): Values for each bit: 1 - IN 0 - OUT open_drain parameter (4 octets / HEX base): Values for each bit: 1 - OPEN pull_on/off parameter (4 octets / HEX base): Values for each bit: 1 - Pull ON 0 - Pull OFF pull_up/down parameter (4 octets / HEX base): Value for each bit: 1 - Pull UP tristate parameter (4 octets / HEX base): Value for each bit: 1 - Tristate	OK	Dev A Dev B
AT+JSLN= <length_friendly_name>, <friendly_name>	**Set Local device friendly Name** Supports all ASCII characters. length_friendly_name parameter (2 octets / DEC base): Length of friendly name, the maximum value for length is 18. friendly_name parameter (length=length_friendly_name): No delimiter is required.	OK	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JPCR= <length_PIN_code>, <PIN_code>	**PIN Code Reply** Sent to PAN1321 in response to a PIN Code Request from a remote Bluetooth device (bd_ addr). length_PIN_code parameter (2 octets / DEC base): Values= 1-16 Length of PIN code PIN_code parameter (length= length_PIN_code): The PIN Code to be sent to the remote Bluetooth device, e.g. AT+JPCR=04,1234 Note: the PIN code is an ACII string.	OK (Followed by): +RPCRCNF=<status> status parameter (1 octet)	Dev A Dev B
AT+JPRO=<mode>	**PROduction mode** mode parameter (1 octet): 1= Production mode ON 0= Production mode OFF	OK	Dev A Dev B
AT+JRBD	**Read Bluetooth device Data** Sent to PAN1321 to retrieve the Bluetooth Device Address and the Oscillator trimming value.	+RRBDRES=<bd_ addr>,< oscTrim> bd_addr parameter (12 octets / HEX base): BD Address of remote device oscTrim parameter (4 octets / HEX base) Oscillator trim value	Dev A Dev B
AT+JRES	**RESet** SW reset of the system.	ROK as applications is restarted.	Dev A Dev B
AT+JRRI	**Read Revision Information**	+RRRICNF=<revision> revision parameter (2 octets / HEX base)	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JRLS=<uuid>, <length_ service_name > <service_name>, <service channel >, <CoD>	**Register Local Service** uuid parameter (4 octets / HEX base): uuid for supported profile e.g.1101 for Serial Port Profile length_service_name parameter (2 octets / DEC base): Values=1-16 Length of service name service_name parameter (length= length_service_name): Name for the service, no final delimiter is needed service channel parameter (2 octets / DEC base): Values range: 0-30 Which service channel to connect to; can be received from a Service Discovery with AT+JSDS CoD parameter (6 octets / HEX base): Class of device. The default CoD value is 000000	OK	Dev B
AT+JRTD=<bd_addr>	**Remove Trusted Device** - deletes the trusted device information for a registered device (bd_addr). bd_addr parameter (12 octets / HEX base): The Bluetooth address of the device that shall be removed from the list	OK	Dev A Dev B
AT+JSCR	**Stream Connection Request** Connects the SPP and UART streams, transparent communication will be enabled if both sides execute this command.	OK	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JSDA=<length>, <data>	**Send Data Request** length parameter (3 octets / DEC base): number of bytes to be sent data parameter (see note for size): data to be sent Note: Maximum number of bytes for each packet is reported at connection confirmation (MTU_ Size) MTU size for PAN1321 is 256 bytes but this parameter is negotiated under connection.	OK	Dev A Dev B
AT+JSDR	**SPP Disconnect Request** Forces an SPP disconnection.	OK	Dev A Dev B
AT+JSDS= <bd_addr>,< uuid>	**Service Discovery Start** Causes PAN1321 to start a service discovery of device with bd_addr and search for services defined by uuid. bd_addr parameter (12 octets / HEX base): BD Address of remote device uuid parameter (4 octets / HEX base): Service to search for e.g. 1101 for Serial Port Profile	OK (Then, if services are returned): +RSDSRES=<remote_ service name>,<remote_ service_channel> remote_service_name parameter (variable length): Name of the remote service. remote_service_ channel parameter (2 octets / DEC base) (For each service) (Completed by): +RSDSCNF=<status> status parameter (1 octet)	Dev A

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JSEC= <security_mode>, <Link_key_information>, <PIN_type>, <length_PIN_code>, <PIN_code>	**Enable SECurity** security_mode parameter (1 octet): 1-Security Mode 1 2-N/A 3-Security Mode 3 (default) link_key_information parameter (1 octet): 1-Inform about link key 2-Don't inform about link key (default) PIN_type parameter (1 octet): 1-Variable PIN 2-Fixed PIN length_PIN_code parameter (2 octets / DEC base): Length of PIN code. The maximum PIN length value is 16 (corresponding to a 16 octets long PIN code) PIN_code parameter (length=length_PIN_code): Normal user PIN, for example "0000" (default), This parameter is taken into account if PIN_ TYPE is fixed. Note: If security mode shall be changed from default settings, AT+JSEC shall be the first command that is sent after a reset. Security mode 3 is the default security mode and the default PIN type is variable.	OK	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
AT+JSNF= <sniff_Max>, <sniff_Min>, <sniff_attempt>, <sniff_tmo>, <on/off>	**Sniff Request** Request a link to enter Sniff Mode. All command parameters are given in HEX base with the exception of on/off parameter. 1 ASCII character represents four bits in HEX base e.g. "A" is 1010. MSB given first. sniff_Max parameter (4 octets / HEX base): Maximum allowed sniff interval Value to be written= N Time = N * 0.625 msec Range: 1.25 msec to 40.9 s sniff_Min parameter (4 octets / HEX base): Minimum allowed sniff interval Value to be written= N Time = N * 0.625 msec Range: 1.25 msec to 40.9 s sniff_attempt parameter (4 octets / HEX base): Number of sniff attempts Value to be written= N Length = N* 1.25 msec Time Range: 0.625msec - 40.9 s sniff_tmo parameter (4 octets / HEX base): The time out value for sniff attempts Value to be written= N Time = N * 0.625 msec Range: 0 msec to 40.9 s on//off parameter (1 octet): One octet to indicate Sniff ON (value=1) or Sniff OFF (value=0)	+RSNFCNF= <sniff_Interval>, <mode> sniff_Interval parameter (4 octets / HEX base): mode parameter (1 octet): One octet to indicate normal mode (mode=0) or sniff mode (mode=2)	Dev A Dev B

Table 6-4

AT Command	Usage	Resulting response(s) from PAN1321	DevA / Dev B
^ ^ ^	**Stream Connection Cancel** End Streaming Mode Send -T0 - ^ -T1- ^ -T1- ^ -T0- with an interval of T1= 1 second between symbols and T0 > 1second. Note: This string is not terminated with CR LF.	OK	Dev A Dev B

6.3.3 AT responses list (not command triggered)

Table 6-5

AT Response	Usage	Command to acknowledge the response	DevA / Dev B
ROK	**Start up response**		Dev A Dev B
+RPCI= <bd_addr>	**Pin Code Indication** bd_addr parameter (12 octets / HEX base): MSB first e.g. 123456789ABC becomes CBA987654321.	AT+JPCR= <length_PIN_code>, <PIN_code> length_PIN_code parameter (2 octets / DEC base): Length of PIN code PIN_code parameter (length=length_PIN_code)	Dev A Dev B
+RCOI= <bd_addr>	**Connect Indication** bd_addr parameter (12 octets / HEX base): See previous response for information on the format.	AT+JACR= <accept> accept parameter (1 octet): 0 - Not accepted 1 - Accepted	Dev B

Table 6-5

AT Response	Usage	Command to acknowledge the response	DevA / Dev B
+RDAI=<length>, <data>	**Data Indication** length parameter (3 octets / DEC base): number of bytes to be sent data parameter (length=length from previous parameter): Received data	Not available during stream mode.	Dev A Dev B
+RDII	**Disconnect Indication**	Received on the side that has not initiated the disconnection.	Dev A Dev B
+RSLE	**Secure Link Established**		Dev A Dev B
+RSNFCNF= <sniff_Interval>, <mode>	**Sniff mode confirmation** sniff_Interval parameter (4 octets / HEX base). mode parameter (1 octet): One octet to indicate Normal mode (mode=0) or sniff mode (mode=2)	Received on the side that has not issued the sniff command (AT+JSNF)	Dev A Dev B

6.4 Example AT commands

Table 6-6

Example: Service Discovery					
Dev A			Dev B		
#	Direction	Command / Event	#	Direction	Command / Event
1	Host <--- PAN1321	ROK			
			2	Host <--- PAN1321	ROK
			3	Host ---> PAN1321	AT+JSEC=1,1,1,04,1111
			4	Host <--- PAN1321	OK
			5	Host ---> PAN1321	AT+JDIS=3
			6	Host <--- PAN1321	OK
			7	Host ---> PAN1321	AT+JRLS=1101,11, Serial Port,01,000000
			8	Host <--- PAN1321	OK
9	Host ---> PAN1321	AT+JSEC=1,,1,1,04,1111			
10	Host <--- PAN1321	OK			
11	Host ---> PAN1321	AT+JSDS=0003199E8B25, 1			
12	Host <--- PAN1321	OK			
13	Host <--- PAN1321	+RSDSRES=Serial Port, 01			
14	Host <--- PAN1321	+RSDSCNF=0			

Table 6-7

Example: Connect (Security mode 3, Default)					
Dev A Security mode 3 (default)			Dev B Security mode 3 (default)		
#	Direction	Command / Event	#	Direction	Command / Event
1	Host <--- PAN1321	ROK			
			2	Host <--- PAN1321	ROK
			3	Host ---> PAN1321	AT+JDIS=3
			4	Host <--- PAN1321	OK
			5	Host ---> PAN1321	AT+JRLS=1101,11,Serial port,01, 000000
			6	Host <--- PAN1321	OK
			7	Host ---> PAN1321	AT+JAAC=1
			8	Host <--- PAN1321	OK
9	Host ---> PAN1321	AT+JCCR= 0003199E8B25,01			
10	Host <--- PAN1321	OK			
11	Host <--- PAN1321	+RPCI=0003199E8B25			
12	Host ---> PAN1321	AT+JPCR=04,0000			
13	Host <--- PAN1321	OK			
			14	Host <--- PAN1321	+RPCI=0003199E8B35
			15	Host ---> PAN1321	AT+JPCR=04,0000
			16	Host <--- PAN1321	OK

Table 6-7

Example: Connect (Security mode 3, Default)					
			17	Host <–– PAN1321	+RSLE
			18	Host <–– PAN1321	+RCOI=0003199E8B35
			19	Host <–– PAN1321	+RCCRCNF=256,0
20	Host <–– PAN1321	+RSLE			
21	Host <–– PAN1321	+RCCRCNF=256,0			

Table 6-8

Example: Connect (Security mode 1, No PIN request)					
Dev A Security mode 1			Dev B Security mode 1		
#	Direction	Command / Event	#	Direction	Command / Event
1	Host <–– PAN1321	ROK			
			2	Host <–– PAN1321	ROK
			3	Host –––> PAN1321	AT+JSEC=1,1,1,04,1111
			4	Host <–– PAN1321	OK
			5	Host –––> PAN1321	AT+JDIS=3
			6	Host <–– PAN1321	OK
			7	Host –––> PAN1321	AT+JRLS=1101, 11, Serial Port, 01, 000000
			8	Host <–– PAN1321	OK
			9	Host –––> PAN1321	AT+JAAC=1
			10	Host <–– PAN1321	OK
11	Host –––> PAN1321	AT+JSEC=1,1,1,04,1111			
12	Host <–– PAN1321	OK			
13	Host –––> PAN1321	AT+JCCR=0003199E8B25 ,01			
14	Host <–– PAN1321	OK			
15	Host –––> PAN1321	+RCCRCNF=256,0			
			16	Host <–– PAN1321	+RCOI=0003199E8B35 +RCCRCNF=256,0

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Limit Values		Unit	Notes
	Min	Max		
Storage temperature	-40	125	°C	-
VSUPPLY supply voltage	-0.3	6.0	V	-
VDDUART supply voltage	-0.9	4.0	V	-
VDD1 supply voltage	-0.9	4.0	V	-
VREG	-0.3	4.0	V	VSUPPLY > 4 V
VREG	-0.3	VSUPPLY	V	VSUPPLY < 4 V
Input voltage range	-0.9	4.0	V	-
Output voltage range	-0.9	4.0	V	-
ESD		1.0	kV	According to MIL-STD883D method 3015.7

Note: Stresses above those listed here are likely to cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.
Maximum ratings are not operating conditions.

7.2 Operating Conditions

Table 7-2 Operating Conditions

Parameter	Limit Values		Unit	Notes
	Min	Max		
Operating temperature	-40	+70	°C	Optional +85°C
VSUPPLY	2.9	4.1[1)]	V	Main supply voltage
VDDUART	1.35	3.63	V	
VDD1	1.35	3.63	V	

1) At ambient temperatures above 65°C the maximum allowed power dissipation in the module is limited to 200 mW

7.3 DC Characteristics

7.3.1 Pad Driver and Input Stages

Table 7-3 Internal1 (1.5 V) supplied Pins (see Chapter 1.5)

Parameter	Condition	Limit Values			Unit
		Min	Typ	Max	
Input low voltage	-	-0.3		0.27	V
Input high voltage	-	1.15		3.6	V
Output low voltage	I_{OL}=1mA			0.25	V
Output high voltage	I_{OH}=-1mA,	1.1			V
Continuous Load[1)]				1	mA
Pin Capacitance				10	pF
Magnitude Pin Leakage	input and output drivers disabled		0.01	1	µA

1) The totaled continuous load for all Internal1 supplied pins shall not exceed 2mA at the same time

Table 7-4 Internal2 (2.5 V) supplied Pins (see Chapter 1.5)

Parameter	Condition	Limit Values			Unit
		Min	Typ	Max	
Input low voltage	-	-0.3		0.45	V
Input high voltage	-P0.10	1.93		2.8	V
	-Other pins	1.93		3.6	V
Output low voltage	I_{OL}=5mA			0.25	V
Output low voltage	I_{OL}=2mA			0.15	V
Output high voltage	I_{OH}=-5mA,	2.0			V
Output high voltage	I_{OH}=-2mA,	2.1			V
Continuous Load[1)]				5	mA
Pin Capacitance				10	pF
Magnitude Pin Leakage	input and output drivers disabled		0.01	1	µA

1) The totaled continuous load for all Internal2 supplied pins shall not exceed 35mA at the same time

Table 7-5 VDDUART supplied Pins (see Chapter 1.5)

Parameter	Condition	Limit Values			Unit
		Min	Typ	Max	
Input low voltage		-0.3		0.2*VDDUART	V
Input high voltage	P0.5/UARTRXD	0.7*VDDUART		VDDUART	V
	Other pins	0.7*VDDUART		3.63	V
Output low voltage	I_{OL}=5mA VDDUART=2.5V			0.25	V
Output low voltage	I_{OL}=2mA VDDUART=2.5V			0.15	V
Output high voltage	I_{OH}=-5mA, VDDUART=2.5V	VDDUART-0.25			V
Output high voltage	I_{OH}=-2mA, VDDUART=2.5V	VDDUART-0.15			V
Continuous Load[1)]				5	mA
Pin Capacitance				10	pF
Magnitude Pin Leakage	input and output drivers disabled		0.01	1	µA

1) The totaled continuous load for all VDDUART supplied pins shall not exceed 35mA at the same time

Table 7-6 VDD1 supplied Pins (see Chapter 1.5)

Parameter	Condition	Limit Values			Unit
		Min	Typ	Max	
Input low voltage		-0.3		0.2*VDD1	V
Input high voltage		0.7*VDD1		3.63	V
Output low voltage	I_{OL}=5mA VDD1=2.5V			0.25	V
Output low voltage	I_{OL}=2mA VDD1=2.5V			0.15	V
Output high voltage	I_{OH}=-5mA, VDD1=2.5V	VDD1-0.25			V
Output high voltage	I_{OH}=-2mA, VDD1=2.5V	VDD1-0.15			V
Continuous Load[1)]				5	mA

Parameter	Condition	Limit Values			Unit
		Min	Typ	Max	
Pin Capacitance				10	pF
Magnitude Pin Leakage	input and output drivers disabled		0.01	1	µA

1) The total continuous load for all VDD1 supplied pins shall not exceed 35mA at the same time

Table 7-7 ONOFF PIN (see Chapter 1.5)

Parameter	Condition	Limit Values			Unit
		Min	Typ	Max	
Input low voltage				0.15[1)]	V
Input high voltage		1.7[1)]		VSUPPLY[1)]	V
Input current	ONOFF=0V	-2[1)]	0.01[1)]	2[1)]	µA
Slew-Rate	When turning ON or OFF	40[1)]			mV/µs

1) Value will be updated after Verification/characterization

7.3.2 Pull-ups and Pull-downs

Table 7-8 Pull-up and pull-down currents

Pin	Pull Up Current			Pull Down Current			Unit	Conditions
	Min	Typ	Max	Min	Typ	Max		
P0.12/SDA0, P0.13/SCL0	260	740	1300	N/A	N/A	N/A	µA	Pull-up current measured with pin voltage = 0V Pull-down current measured with pin voltage = supply voltage Min measured at 125°C with supply = 1.35V Typ measured at 27°C with supply = 2.5V Max measured at -40°C with supply = 3.63V
TRST#, JTAG#, P0.0, P0.1, P0.2, P0.3	22	130	350	23	150	380	µA	
P0.4/UARTTXD, P0.5/UARTRXD, P0.6/UARTRTS, P0.7/UARTCTS, P0.10, P0.8, P0.9, P0.11 P0.14, P0.15/SLEEPX	4.2	24	68	3.0	20	55	µA	
P1.0/TMS, P1.1/TCK, P1.2/TDI, P1.3/TDO, P1.4/RTCK, P1.5/CLK32, P1.6, P1.7, P1.8	1.1	6.0	17	0.75	5.0	14	µA	

7.3.3 Protection Circuits

All pins have an inverse protection diode against VSS.
P0.10 has an inverse diode against Internal2.
P0.5/UARTRXD has an inverse diode against VDDUART.
All other pins have no diode against their supply.

7.4 System Power Consumption

Table 7-9 Current Consumption In Different Operating Modes

This table shows the Vsupply current consumption. All I/O current is neglected since they depend mainly on the external load.

T=25°C, Output Power=0dBm,

Parameters	Min	Typ	Max	Unit	Comment
Ultra Low Power Mode		30		µA	VDDPM from internal regulator
Page & Inquiry Scan (1.28s)		0.89		mA	
Sniff (1.28s)		0.20		mA	
ACL (Transmit DH1)		38		mA	Basic Rate, 179.2 kb/s[1)]
ACL (Receive DH1)		35		mA	Basic Rate, 179.2 kb/s[1)]
ACL (Transmit 2-DH1)		40		mA	Enhanced Data Rate, 345.6 kb/s[1)]
ACL (Receive 2-DH1)		37		mA	Enhanced Data Rate, 345.6 kb/s[1)]
ACL (Transmit 3-DH1)		40		mA	Enhanced Data Rate, 531.2 kb/s[1)]
ACL (Receive 3-DH1)		37		mA	Enhanced Data Rate, 531.2 kb/s[1)]
SCO (HV3)		19		mA	

1) Figure indicates maximum possible data rate with this packet type

Table 7-10 Max. Load at the Different Supply Voltages

I/O currents are not included since they depend mainly on external loads.

Parameters	Min	Typ	Max	Unit	Comment
Vsupply			100	mA	peak current

7.5 AC Characteristics

7.5.1 Characteristics of 32.768 kHz Clock Signal

The 32.768 kHz clock signal applied to CLK32 must be a rectangular waveform with a duty cycle of between 10-90%. The frequency accuracy must be better than 250 ppm. The rise and fall time of the signal must be less than 10 µs.

7.6 RF Part

7.6.1 Characteristics RF Part

The characteristics involve the spread of values to be within the specific temperature range. Typical characteristics are the median of the production.

All values refers to Infineon reference design. All values will be updated after verification/ Characterisation.

7.6.1.1 Bluetooth Related Specifications

Table 7-11 BDR - Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output power (high gain)	0.5	2.5	4.5	dBm	Default settings
Output power (highest gain)		4.5		dBm	Maximum settings
Power control step size	4	6	8	dB	
Frequency range fL	2400	2401.3		MHz	
Frequency range fH		2480.7	2483.5	MHz	
20dB bandwidth		0.930	1	MHz	
2nd adjacent channel power		-40	-20	dBm	
3rd adjacent channel power		-60	-40	dBm	
>3rd adjacent channel power		-64	-40	dBm	max. 2 of 3 exceptions @ 52 MHz offset might be used
Average modulation deviation for 00001111 sequence	140	156	175	kHz	
Minimum modulation deviation for 01010101 sequence	115	145		kHz	
Ratio Deviation 01010101 / Deviation 00001111	0.8	1			
Initial carrier frequency tolerance |foffset|			75	kHz	
Carrier frequency drift (one slot) |fdrift|		10	25	kHz	
Carrier frequency drift (three slots) |fdrift|		10	40	kHz	
Carrier frequency drift (five slots) |fdrift|		10	40	kHz	

Table 7-11 BDR - Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Carrier frequency driftrate (one slot) |fdriftrate|		5	20	kHz/ 50µs	
Carrier frequency driftrate (three slots) |fdriftrate|		5	20	kHz/ 50µs	
Carrier frequency driftrate (five slots) |fdriftrate|		5	20	kHz/ 50µs	

Table 7-12 BDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Sensitivity		-86	-81	dBm	ideal wanted signal
C/I-performance: -4th adjacent channel		-51	-40	dB	
C/I-performance: -3rd adjacent channel (1st adj. of image)		-46	-20	dB	
C/I-performance: -2nd adjacent channel (image)		-35	-9	dB	
C/I-performance: -1st adjacent channel		-4	0	dB	
C/I-performance: co. channel		9	11	dB	
C/I-performance: +1st adjacent channel		-4	0	dB	
C/I-performance: +2nd adjacent channel		-40	-30	dB	
C/I-performance: +3rd adjacent channel		-50	-40	dB	
Blocking performance 30MHz-2GHz	10			dBm	some spurious responses, but according to BT-specification
Blocking performance 2GHz-2.4GHz	-27			dBm	
Blocking performance 2.5GHz-3GHz	-27			dBm	

Table 7-12 BDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Blocking performance 3GHz-12.75GHz	10			dBm	some spurious responses, but according to BT-specification
Intermodulation performance	-39	-34		dBm	valid for all intermodulation tests
Maximum input level	-20			dBm	

Table 7-13 EDR - Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output power (high gain)	-2	0	2	dBm	
Relative transmit power: PxPSK - PGFSK	-4	-0.6	1	dB	
Carrier frequency stability |ωi|			75	kHz	
Carrier frequency stability |ωi+ω0|			75	kHz	
Carrier frequency stability |ω0|		2	10	kHz	
DPSK - RMS DEVM		10	20	%	
8DPSK - RMS DEVM		10	13	%	
DPSK - Peak DEVM		20	35	%	
8DPSK - Peak DEVM		20	25	%	
DPSK - 99% DEVM			30	%	
8DPSK - 99% DEVM			20	%	
Differential phase encoding	99	100		%	
1st adjacent channel power		-40	-26	dBc	
2nd adjacent channel power			-20	dBm	Carrier power measured at basic rate.
≥3rd adjacent channel power			-40	dBm	Carrier power measured at basic rate.

Table 7-14 EDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
DQPSK-Sensitivity		-88	-83	dBm	ideal wanted signal
8DPSK-Sensitivity		-83	-78	dBm	ideal wanted signal
DQPSK - BER Floor Sensitivity		-84	-60	dBm	
8DPSK - BER Floor Sensitivity		-79	-60	dBm	
DQPSK - C/I-performance: -4th adjacent channel		-53	-40	dB	
DQPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		-47	-20	dB	
DQPSK - C/I-performance: -2nd adjacent channel (image)		-31	-7	dB	
DQPSK - C/I-performance: -1st adjacent channel		-7	0	dB	
DQPSK - C/I-performance: co. channel		11	13	dB	
DQPSK - C/I-performance: +1st adjacent channel		-9	0	dB	
DQPSK - C/I-performance: +2nd adjacent channel		-44	-30	dB	
DQPSK - C/I-performance: +3rd adjacent channel		-50	-40	dB	
8DPSK - C/I-performance: -4th adjacent channel		-48	-33	dB	
8DPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		-44	-13	dB	
8DPSK - C/I-performance: -2nd adjacent channel (image)		-25	0	dB	
8DPSK - C/I-performance: -1st adjacent channel		-5	5	dB	
8DPSK - C/I-performance: co. channel		17	21	dB	
8DPSK - C/I-performance: +1st adjacent channel		-5	5	dB	
8DPSK - C/I-performance: +2nd adjacent channel		-36	-25	dB	

Table 7-14 EDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
8DPSK - C/I-performance: +3rd adjacent channel		-46	-33	dB	
Maximum input level	-20			dBm	

8 Package Information

8.1 Package Marking

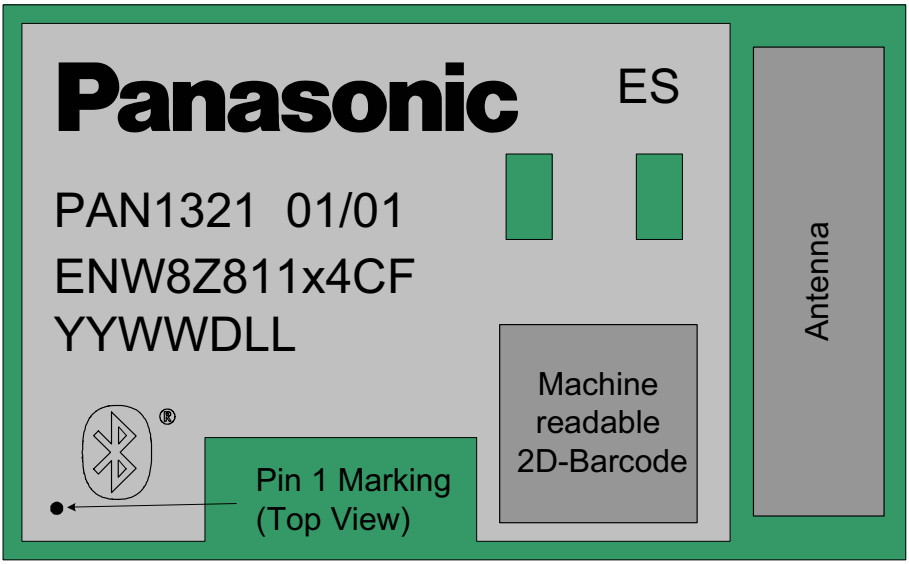


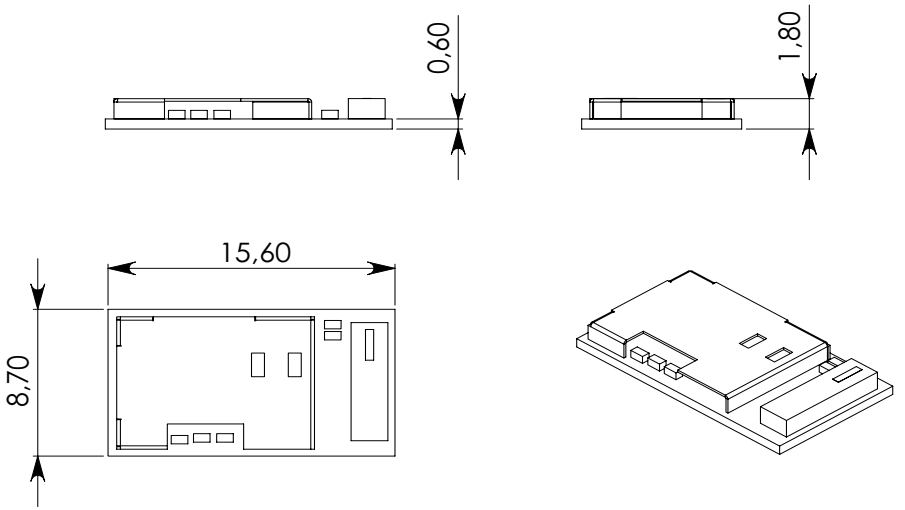
Figure 8-1 PAN1321 Top View

Table 8-1 Marking Explanation

Marking	Remark
PAN1321	Product Name
01/01	Revision Hardware/Software[1)]
ENW8Z811x4CF	Ordering Code please refer to **Chapter 1.2**
ES	Engineering Sample, no mass production product now
YYWWDLL	Date Code

1) This is only related to the BD Data values for the EEPROM.

8.2 Production Package



All dimensions are in mm.

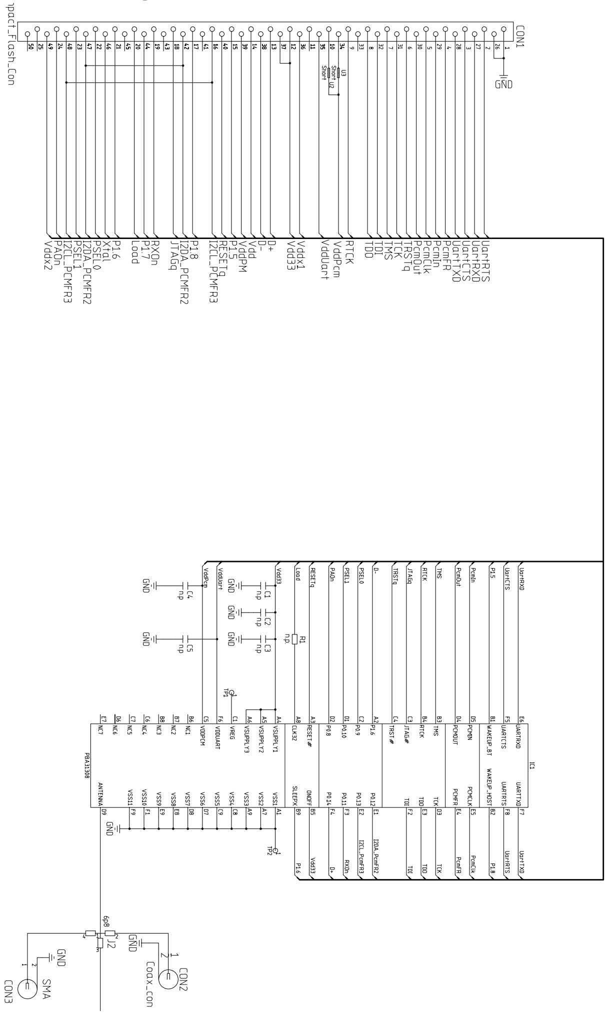
Tolerances on all outer dimensions, height, width and length, are +/- 0.2 mm.

9 Reference Schematics

This section contains reference schematics for PAN1321.

9.1 Reference design

Figure 9-1 Reference design schematics



10 Assembly Guideline

The target of this section is to provide guidelines for customers to successfully introduce the PAN1321 module in production. This includes general description, PCB-design, solder printing process, assembly, soldering process, rework and inspection.

10.1 General description of the module

PAN1321 is a Land Grid Array (LGA 11,6 mm x 8,7 mm) module made for surface mounting. The pad diameter is 0.6 mm and the pitch 1.2 mm.

All solder joints on the module will reflow during soldering on the mother board. All components and shield will stay in place due to wetting force.

Surface treatment on the module pads is Nickel (5-8 µm)/Gold (0.04-0.10 µm).

Figure 10-1 shows the pad layout on the module, seen from component side.

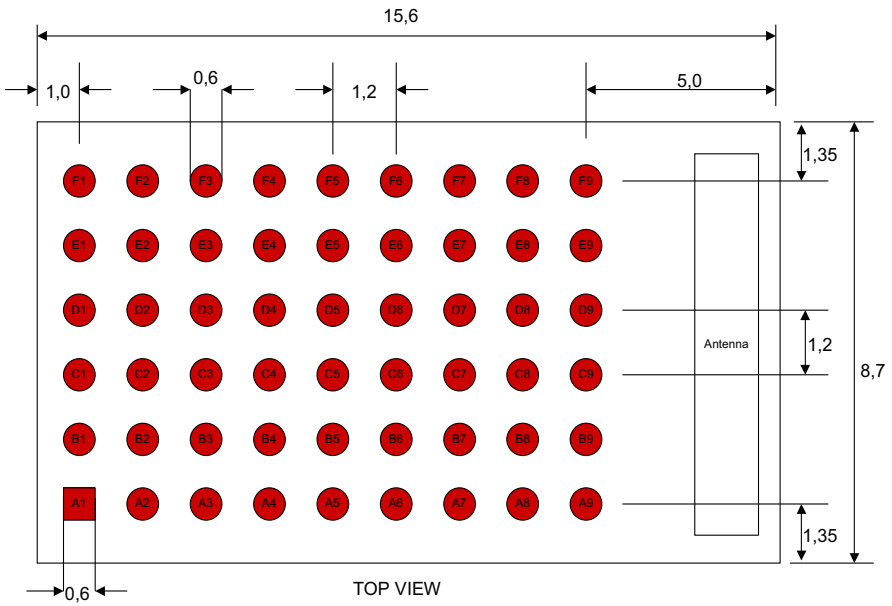


Figure 10-1 Pad layout on the module (top view).

10.2 Printed Circuit Board design

The land pattern on the PCB shall be according to the land pattern on the module, which means that the diameter of the LGA pads on the PCB shall be 0.6 mm. It is recommended that each pad on the PCB shall be surrounded by a solder mask clearance of about 75 µm to avoid overlapping solder mask and pad.

10.3 Solder paste printing

The solder paste deposited on the PCB by stencil printing has to be of eutectic or near eutectic tin leadfree / lead composition. A no-clean solder paste is preferred, since cleaning of the solder joints is difficult because of the small gap.

Preferred thickness of the solder paste stencil is 100 - 127 µm (4 - 5 mils). The apertures on the solder paste stencil shall be of the same size as the pads, 0.6 mm.

10.4 Assembly

10.4.1 Component placement

In order to assure a high yield, good placement on the PCB is necessary. As a rule of thumb the tolerable misplacement is 150 µm. This means that the PAN1321 module can be assembled with a variety of placement systems.

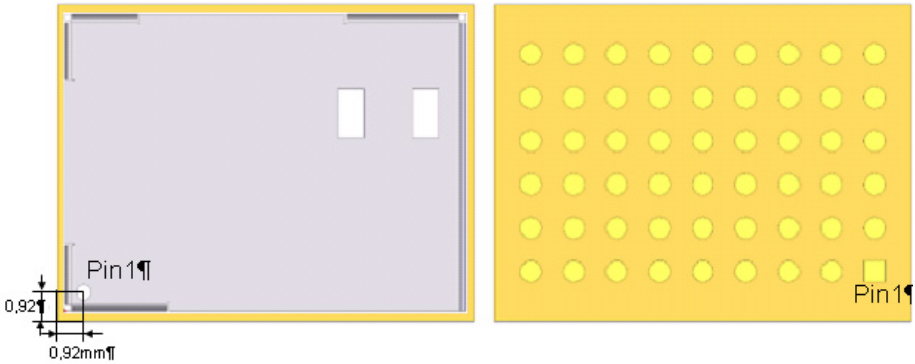
It is recommended to use a vision system capable of package pad recognition and alignment that evaluates the pad locations on the package (in contrast to outline centring). This eliminates the pad to package edge tolerance.

The recommendation is to pick and place the module with a nozzle in the centre of the shield. The nozzle diameter shall not be bigger than 4 mm.

10.4.2 Pin mark

Pin 1 (A0) is marked on bottom footprint and on the top of the shield on the module according to **Figure 10-2**. Diameter of pin 1 mark on the shield is 0.40 mm.

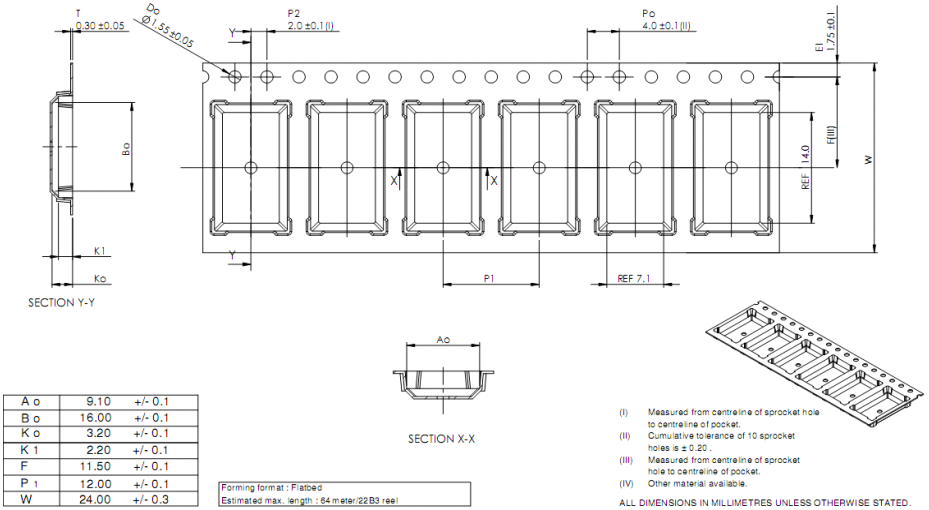
Figure 10-2 Topview and bottom view



10.4.3 Package

PAN1321 is packed in tape on reel according to **Figure 10-3**.

Figure 10-3 Tape and reel



A o	9.10	+/- 0.1
B o	16.00	+/- 0.1
K o	3.20	+/- 0.1
K 1	2.20	+/- 0.1
F	11.50	+/- 0.1
P 1	12.00	+/- 0.1
W	24.00	+/- 0.3

10.5 Solder Profile

Generally all standard reflow soldering processes (vapour phase, convection, infra red) and typical temperature profiles used for surface mount devices are suitable for the PAN1321 module. Wave soldering is not possible. **Figure 10-4** and **Figure 10-5** shows example of a suitable solder reflow profile. One for leaded and one for leadfree solder.

At the reflow process each solder joint has to be exposed to temperatures above solder liquids for a sufficient time to get the optimum solder joint quality, whereas overheating the board with its components has to be avoided. Using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB (especially on large, complex boards with different thermal masses of the components). The most recommended types are therefore forced convection or vapour phase reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary.

The reflow profiles and other reflow parameters are dependent on the used solder paste. The paste manufacturer provides a reflow profile recommendation for this product.

Additionally it is important not to overheat the PAN1321 module by a too large reflow peak temperature. PAN1321 contain several plastic packages and is there by sensitive of the moisture content level at the time of board assembly.

Overheating in combination with excessive moisture content could result in package delaminations or cracks (popcorn effect). The heating rate should not exceed 3°C/s and max sloping rate should not exceed 4°C/s.

PAN1321 shall be handled according to MSL3, which means a floor life of 168 h in 30°C/ 60% r.h.

Figure 10-4 Eutectic Lead-Solder Profile

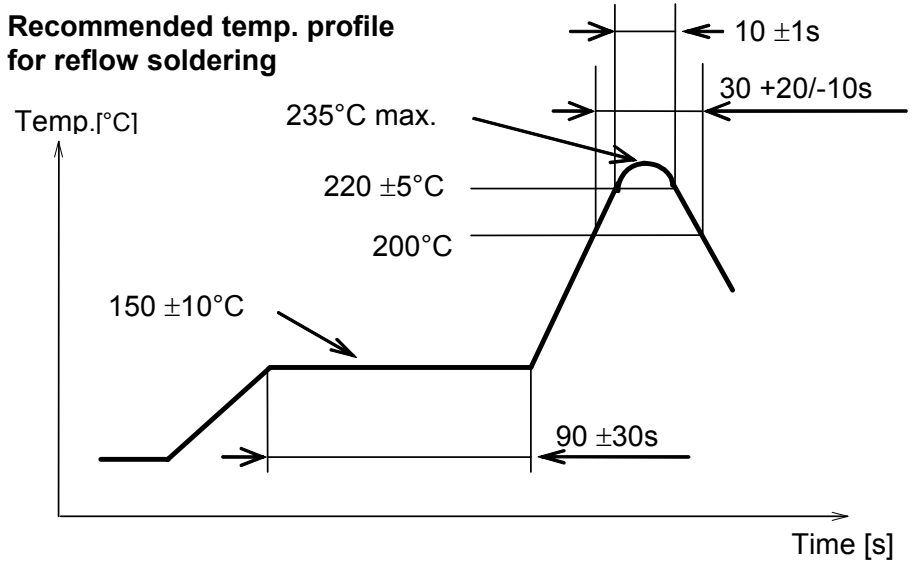
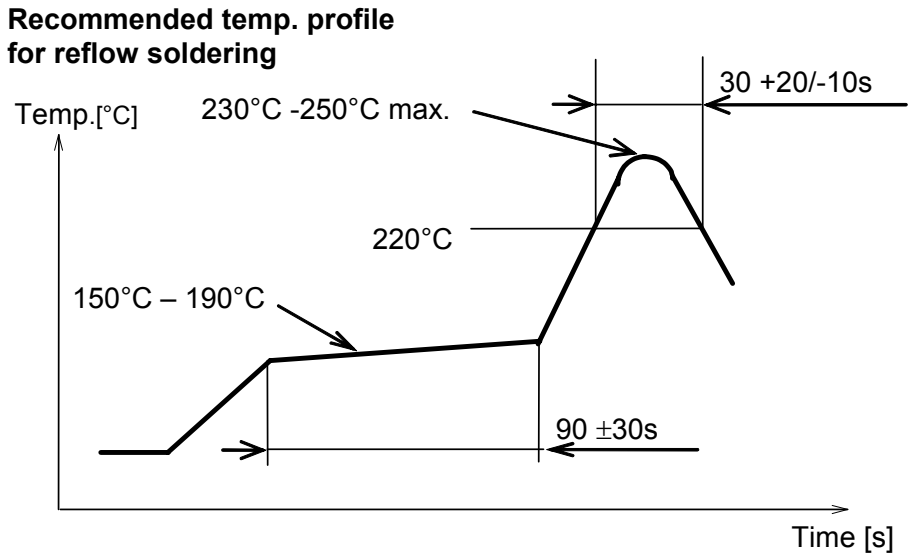


Figure 10-5 Eutectic Leadfree-Solder Profile



10.6 Inspection

Automatic inspection of the solder paste printing before assembly is highly recommended to ensure high yield and good long term reliability.

10.7 Component salvage

If it is intended to send a defect PAN1321 module back to the supplier for failure analysis, please note that during the removal of this component no further defects must be introduced to the device, because this may hinder the failure analysis at the supplier. This includes ESD precautions, not to apply high mechanical force for component removal, and to prevent excess moisture content in the package during salvage (risk of pop corning failures). Therefore if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried 24h at 125°C before soldering off the defect component, because otherwise too much moisture may have been accumulated.

11 Acronyms & Abbreviations

Table 1

Acronym or abbreviation	Writing out in full
ACK	Acknowledgement
ACL	Asynchronous Connection-oriented (logical transport)
AFH	Adaptive Frequency Hopping
AHS	Adaptive Hop Sequence
ARQ	Automatic Repeat reQuest
b	bit/bits (e.g. kb/s)
B	Byte/Bytes (e.g. kB/s)
BALUN	BALanced UNbalanced
BD_ADDR	Bluetooth Device Address
BER	Bit Error Rate
BMU	BlueMoon Universal
BOM	Bill Of Material
BT	Bluetooth
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
COD	Class Of Device
CODEC	COder/DECoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CTS	Clear To Send (UART flow control signal)
CVSD	Continuous Variable Slope Delta (modulation)
DC	Direct Current
DDC	Device Data Control
DM	Data Medium-Rate (packet type)
DMA	Direct Memory Access
DH	Data High-Rate (packet type)
DPSK	Differential Phase Shift Keying (modulation)
DQPSK	Differential Quaternary Phase Shift Keying (modulation)
DSP	Digital Signal Processor

Table 1

Acronym or abbreviation	Writing out in full
DUT	Device Under Test
CDCT	Clock Drift Compensation Task
CQDDR	Channel Quality Driven Data Rate
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended Synchronous Connection-Oriented (logical transport)
EV	Extended Voice (packet type)
FEC	Forward Error Correction
FHS	Frequency Hop Synchronization (packet)
FIFO	First In First Out (buffer)
FM	Frequency Modulation
FW	Firmware
GFSK	Gaussian Frequency Shift Keying (modulation)
GPIO	General Purpose Input/Output
GSM	Global System for Mobile communication
HCI	Host Controller Interface
HCI+	Infineon Specific HCI command set
HEC	Header Error Check
HV	High quality Voice (packet type)
HW	Hardware
I2C	Inter-IC Control (bus)
I2S	Inter-IC Sound (bus)
IAC	Inquiry Access Code
ID	IDentifier
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ISM	Industrial Scientific & Medical (frequency band)
JTAG	Joint Test Action Group
LAN	Local Area Network
LAP	Lower Address Part
LM	Link Manager
LMP	Link Manager Protocol

Table 1

Acronym or abbreviation	Writing out in full
LNA	Low Noise Amplifier
LO	Local Oscillator
LPM	Low Power Mode(s)
LPO	Low Power Oscillator
LSB	Least Significant Bit/Byte
LT_ADDR	Logical Transport Address
MSB	Most Significant Bit/Byte
MSRS	Master-Slave Role Switch
NC	No Connection
NOP	No OPeration
NVM	Non-Volatile Memory
OCF	Opcode Command Field
OGF	Opcode Group Field
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Coded Modulation
PDU	Protocol Data Unit
PER	Packet Error Rate
PIN	Personal Identification Number
PLC	Packet Loss Concealment
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power-On Reset
PTA	Packet Traffic Arbitration
PTT	Packet Type Table
QoS	Quality Of Service
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send (UART flow control signal)
RX	Receive

Table 1

Acronym or abbreviation	Writing out in full
RXD	Receive Data (UART signal)
SCO	Synchronous Connection-Oriented (logical transport)
SIG	Special Interest Group (Bluetooth SIG)
SW	Software
SYRI	Synthesizer Reference Input
TBD	To Be Determined
TCK	Test Clock (JTAG signal)
TDI	Test Data In (JTAG signal)
TDO	Test Data Out (JTAG signal)
TL	Transport Layer
TMS	Test Mode Select (JTAG signal)
TX	Transmit
TXD	Transmit Data (UART signal)
UART	Universal Asynchronous Receiver & Transmitter
ULPM	Ultra Low Power Mode
VCO	Voltage Controlled Oscillator
WLAN	Wireless LAN (Local Area Network)

12 References

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