NEW

# Radiometrix

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**Issue 1, 20 May 2009** **DWA3**

## Transparent Data Link on 868/914MHz band

***A DWA3 is a single channel, 869 or 915MHz wideband, transparent data link. It has a TDL2A pin out (and firmware), but uses a BiM3 series radio module. DWA3 acts as a transparent serial cable to attached host. DWA3 is an intermediate level OEM radio modem which is in between a raw FM radio module like BiM3A/BiM3B and a sophisticated OEM radio modem like RPM3. It takes care of preamble, synchronisation, bit balancing and error checking along with automatic noise squelching.***


*Figure 1: DWA3-868.30-9 radio modem*

The DWA3 provides a half duplex link. Provided no two devices attempt to transmit simultaneously no further restrictions on data transmission need be made, as all transmit timing, valid data identification and datastream buffering is conducted by the unit. Synchronisation and framing words in the packet prevent the receiver outputting garbage in the absence of wanted RF signal or presence of interference. For multiple radio systems (polled networks) a DWA3 can be set to 1 of 8 unique addresses.



### Features

- Conforms to EN 300 220-3 and EN 301 489-3
- Crystal controlled PLL FM circuitry for both Tx and Rx
- Built-in ceramic patch antenna
- SAW front-end filter
- Single conversion superhet
- Serial modem baud rate at 9600bps (half-duplex)
- Addressable point-to-point

### Applications

- PDAs, organisers & laptops
- Handheld / portable terminals
- EPOS equipment, barcode scanners
- In-building environmental monitoring and control
- Remote data acquisition system, data logging
- Fleet management, vehicle data acquisition

### Technical Summary

- Operating frequency: 869.85 /868.30MHz (Europe), 914.5MHz (North America)
- Modulation: 16kbps bi-phase FSK
- Supply: 5V at 18mA transmit (@5mW), 15mA receive/idle
- Transmit power: +5mW @ 869.85MHz
- Receiver sensitivity: -106dBm (for 1% BER)
- 32 byte data buffer

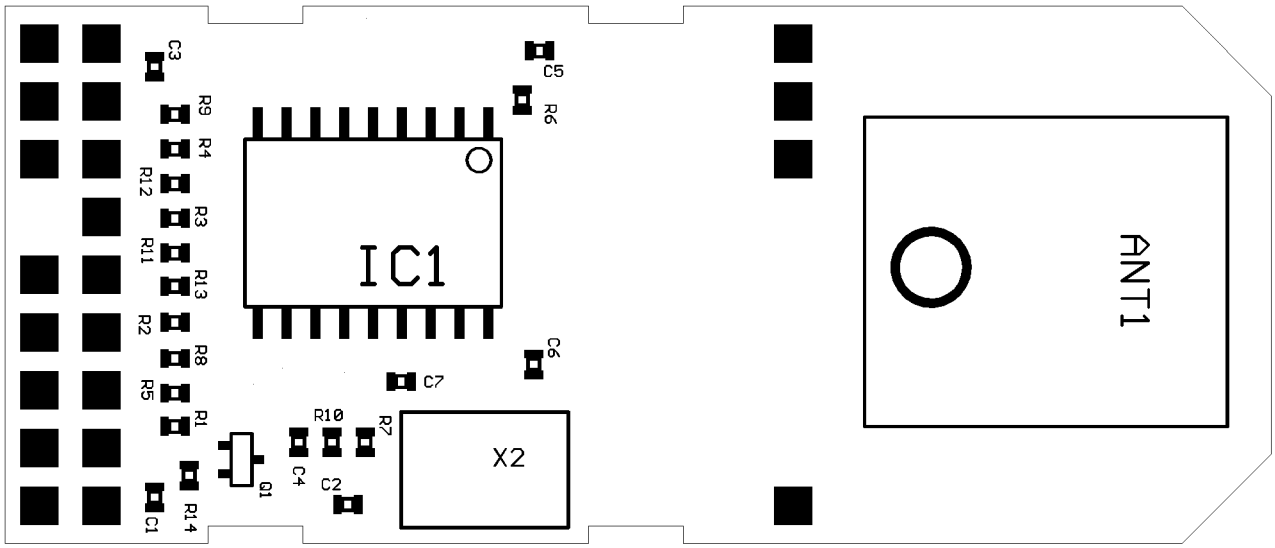


***Figure 2: DWA3 footprint (top view)***

***Pin description***

| Pin | Name | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | Vcc | 5V regulated power supply (4.75 - 5.25v) |
| 3 | $\overline{\text{ENABLE}}$ | Pull low to enable module |
| 4 | $\overline{\text{SETUP}}$ | Pull low to enter Test/Setup mode (5V CMOS logic. Pull up to 5V) |
| 5 | TXD | Transmit Data (Inverted RS232 in at 5V CMOS logic, No pullup) |
| 6 | NC | No Pin |
| 7 | RXD | Receive Data (Inverted RS232 output at 5V CMOS logic output) |
| 8 | STATUS | RX Busy, Data in receive buffer (5V CMOS logic output) |
| 9 | GND | Ground |

**NOTE**:
1. ENABLE and SETUP have 10K pullups to Vcc. TXD has none (if used in RX only, tie this pin to +5v)
2. Vcc must be a 5v regulated supply (4.75 - 5.25v)
3. Pinout is as TDL2A. (It is, however, longer than 33mm, with a ceramic patch antenna replacing the RF pins)
3. TXD / RXD are inverted RS232 at 5v cmos levels. To connect to a true RS232 device, inverting level shifters must be used (MAX232 type are ideal, but simple NPN transistor switches with pullups often suffice). With typical microcontrollers and uarts, direct connection is possible.
3a DWA3 is compatible with the TDi2 interface board (which provides a MAX232 type buffer, 9 way D connector, 5v voltage regulator and support circuits) provided the SMA RF connector is not fitted. This board is 61mm x 33mm in size.
4. Rx_busy pin goes high when valid data is present in the receive buffer.
5. The DWA3 provides a half duplex link, but provided no two devices attempt to transmit at one time (a 'low' on RX_busy may be used as a primitive 'CTS' indication) no further restrictions on data transmission need be made, as all transmit timing, valid data identification and datastream buffering is conducted by the unit. There is no 'transmit enable' pin.
Sync and framing words in the packet prevent the receiver outputting garbage in the absence of signal or presence of interference.
6. A simple addressing structure is included in the datastream. Units may be programmed onto one of eight addresses (all units are supplied set to default addr=0)
7. DWA3 uses a BiM3 series transceiver module (e.g. BiM3A-914-64, BiM3B-869-64) and the cpu circuitry of the TDL3F
8. This unit is programmed exactly as a TDL2A, with the channel select commands being ignored.

## Serial interface – modem operation

To connect to a true RS232 device, inverting RS232-CMOS level shifters must be used. Maxim MAX232 or equivalent are ideal, but simple NPN transistor switches with pull-ups often suffice. With typical microcontrollers and UARTs, direct connection is possible.

### *The Radio / data stream interface*

A 32 byte software FIFO is implemented in both the transmit and receive sub-routine. At the transmitting end this is used to allow for the transmitter start up time (about 4mS), while on receiving end it buffers arriving packets to the constant output data rate. All timing and data formatting tasks are handled by the internal firmware. The user need not worry about keying the transmitter before sending data as the link is entirely transparent.

For transmission across the radio link data is formatted into packets, each comprising 3 bytes of data and a sync code. If less than 3 bytes are in the transmit end FIFO then a packet is still sent, but idle codes replaces the unused bytes. When the transmit end FIFO is completely emptied, then the transmitter is keyed off.

### *Operation: Radio interface*.

Raw data is not fed to the radios. A coding operation in the transmit sub-routine, and decoding in the receiver, isolate the AC coupled, potentially noisy baseband radio environment from the datastream.

The radio link is fed a continuous tone by the modem. As in bi-phase codes, information is coded by varying the duration consecutive half-cycles of this tone. In our case half cycles of 62.5us and 31.25us are used. In idle (or 'preamble') state, a sequence of the longer cycles is sent (resembling an 8KHz tone).

A packet comprises the Synchronising (or address) part, followed by the Data part, made up of twelve Groups (of four half cycles duration). Each Group encodes 2 data bits, so one byte is encoded by 4 Groups.

## Programming the DWA3

In order to use all the functions embedded in the DWA3, the user must be aware of the setup/programming facility, which allow different addresses and frequency channels to be set up, and if necessary accesses diagnostic test modes.

The DWA3 is programmed through the same RS232 port that is used for sending/receiving data. An RS232 terminal emulator (such as Aterm or HyperTerminal) is an ideal tool.

To enter program mode, the **SETUP pin** must be **pulled low**. In this mode the radio link is disabled, but characters sent (at 9600 baud, as normal) to the unit are echoed back on the RXD pin.

*The unit will only respond to certain command strings*:

**ADDR0** to **ADDR7** <CR>: These commands set up one of 8 unique addresses.

A DWA3 will only communicate with a unit set to the same address.

Address and channel numbers are stored in volatile memory. On power-up the DWA3 reverts to the default in EEPROM (as supplied this is always address 0)

**SETPROGRAM** <CR>: Writes the current address and current channel into EEPROM as the new default.
A tilda character (~, ascii 126dec) sent by the unit indicates end of EEPROM write sequence

(these commands are normally only used for factory diagnostics)
**NOTONE** <CR>: Transmit unmodulated carrier
**LFTONE** <CR>: Transmit carrier modulated with 8KHz squarewave
**HFTONE** <CR>: Transmit carrier modulated with 16KHz squarewave
**#** <CR>: Transmitter off

A Carriage Return '<CR>' (00Dhex) should be entered after each command sequence to execute it.

Releasing the SETUP pin to high state returns the DWA3 to normal operation.

## Interfacing a microcontroller to DWA3

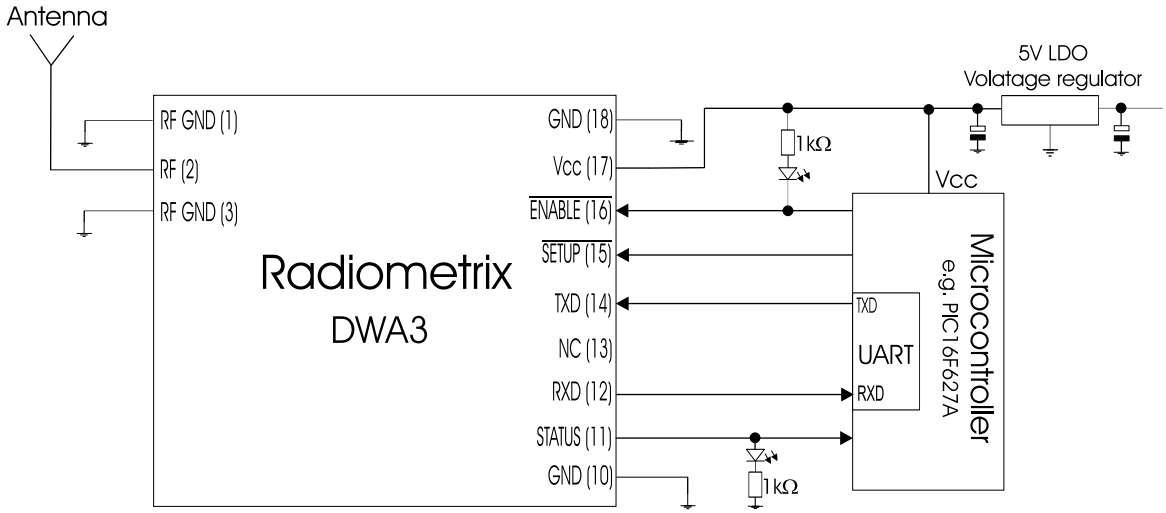


***Figure 5: DWA3 interfaced directly to a microcontroller***

DWA3 can be directly interfaced to any microcontrollers. If the microcontroller has a built-in UART, it can concentrate on its main task and leave the packet formatting, bit balancing and error checking of serial data to DWA3.

Serial data should be in the following format:

1 start bit, 8 data bits, no parity, 1 or 2 stop bits
9600bps
0V=low, 5V=high

STATUS pin can be connected to one of the port pins which can generate an interrupt on low-to-high transition (e.g. RB0/INT pin in the PIC). This can be used to enter a receive sub-routine to download data received from remote DWA3. Therefore, the host does not need to wait in a loop for a packet.

Range test and site survey can be carried out by connecting an LED on the STATUS pin. Every time, DWA3 is within range to receive valid data, the LED will flicker.

## Interfacing DWA3 to an RS232 port

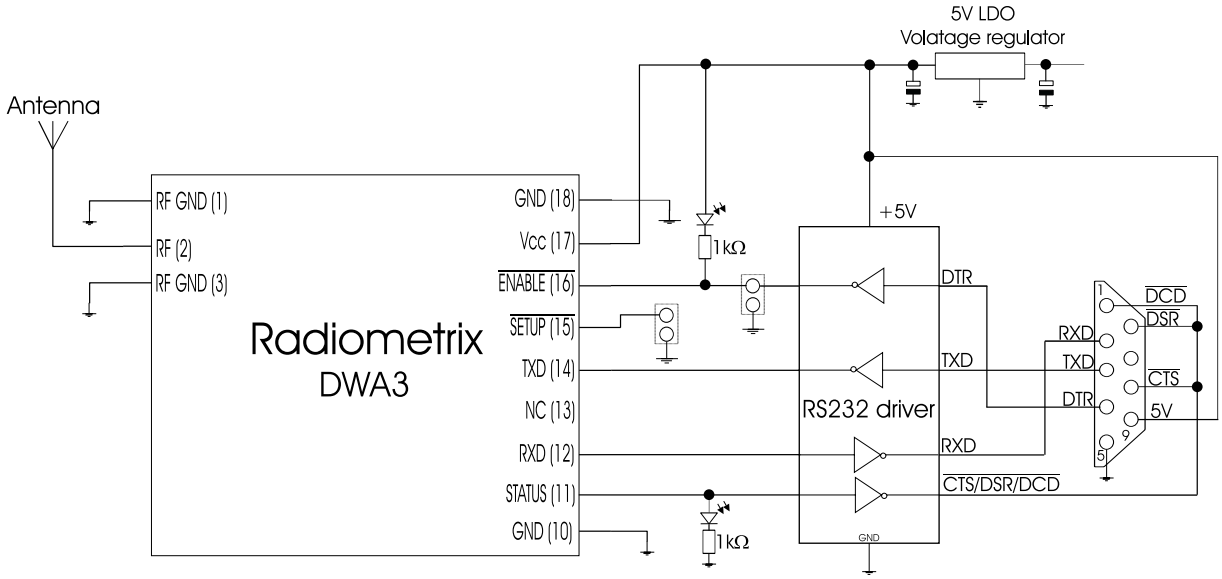


***Figure 6: DWA3 interfaced to an RS232 port via an RS232 line driver/receiver***

STATUS pin in this can be connected to CTS, DSR and DCD pin to simulate a flow control signal.

DWA3 is capable of continuously streaming data at 9600bps. Therefore, STATUS pin is not asserted to stop the Host from sending data as in normal RTS/CTS flow control method, but merely to warn the host that there is already data in the receive buffer which need to be downloaded before sending any more data.

Some DTE hosts assert DTR signal when they are active and this can be used via RS232 line receiver to enable DWA3. Otherwise the ENABLE must be physically pulled-low to activate the DWA3.

***NOTE:***
An interface board (with MAX232 type buffer, 9 way D connector, 5V voltage regulator and SMA RF connector) is available. This board is 61mm x 33mm in size.

## Condensed specifications

| | | |
|---|---|---|
| **Frequency** | | 868.30MHz or 869.85MHz (Europe)<br>914.5MHz (North America) |
| | *Frequency stability* | ±25kHz |
| | *Channel width* | 400kHz |
| | *Number of channels* | 1 |
| **Supply** | *Voltage* | 5V |
| | *Current Transmit* | 40mA @ 868.30MHz, 18mA @ 869.85MHz, 12mA @ 914.5MHz |
| | *Receive/idle* | 15mA |
| Operating temperature | | -20 ˚C to +70 ˚C (Storage -30 ˚C to +70 ˚C) |
| Spurious radiations | | Compliant with ETSI EN 300 220-3 and EN 301 489-3 and FCC Part 15 |
| **Interfaces** | | |
| | *User* | 9pin 0.1" pitch molex (pin 6 absent) |
| | *RF* | Phycomp 431111900087 wideband ceramic antenna |
| Size | | 56 x 23 x 10mm |

| | |
|---|---|
| ***Transmitter*** | |
| Output power | 25mW @ 868.30MHz<br>5mW @ 869.85MHz<br>-1dBm (0.75mW) @ 914.5MHz |
| Duty cycle limit | 1% @ 868.30MHz<br>100% @ 869.85MHz<br>100% @ 914.5MHz |
| TX on switching time | <4ms |
| Modulation type | 16kbps bi-phase FSK |
| FM peak deviation | +/-40KHz (typ.) |
| TX spurious | <-40dBm |
| | |
| ***Receiver*** | |
| Sensitivity | -106dBm for 1% BER |
| spurious / adjacent channel | -50dB |
| LO re-radiation | <-100dBm typ. |
| | |
| ***Interface*** | |
| Data rate | 9600baud, Half duplex |
| Format | 1 start, 8 data, 1 stop, no parity |
| Levels | 5V CMOS (inverted RS232. Mark = 5V = idle) |
| Buffers | 32 byte FIFO |
| Flow control | None ('RX busy' pin provided) |
| Addressing | 1 of 8, user programmed |
| | |
| Data latency | 14ms (first byte into TX, to first byte out of RX) |



### *Ordering information*

The DWA3 radio modem is manufactured in the following variants as standard:

| Part Number | Frequency band | RF power (typ.) | Baud rate |
|---|---|---|---|
| DWA3-869.85-9 | 869.85 MHz | 5mW | 9.6kbps |
| DWA3-868.30-9 | 868.30 MHz | 25mW | 9.6kbps |
| DWA3-914.50-9 | 914.50 MHz | 1mW | 9.6kbps |

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The Intrastat commodity code for all our modules is: 8542 6000.

## *R&TTE Directive*

After 7 April 2001 the manufacturer can only place finished product on the market under the provisions of the R&TTE Directive. Equipment within the scope of the R&TTE Directive may demonstrate compliance to the essential requirements specified in Article 3 of the Directive, as appropriate to the particular equipment.
Further details are available on The Office of Communications (Ofcom) web site:

***http://www.ofcom.org.uk/radiocomms/ifi/***

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