Radiometrix



OR96

27 February 2008

Hartcran House, 231 Kenton Lane, Harrow, HA3 8RP, England Tel: +44 (0) 20 8909 9595, Fax: +44 (0) 20 8909 2233

9600 Baud Quasi DC Data Recovery Module

The Quasi DC Recovery circuit (QR96) can be used to improve data recovery of receiver if the raw data is transmitted without any bit balancing. The QR96 measures the minimum and maximum levels of the AF output of the receiver, averages that and compares the original AF output signal with it. The module can be used in applications where raw (non-bit balanced) data need to be transmitted and received between two UARTs.

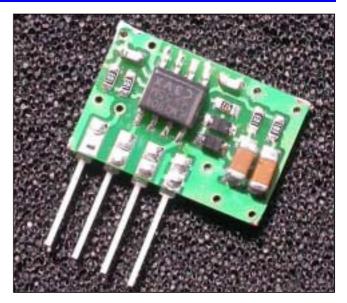


Figure 1: QR96

Features

- Recovery of data signals with frequencies down to 2Hz
- Tolerates time between bit transitions as long as 250ms
- Permits non-bit balanced data stream like straight ASCII
- Improves link margin by about 6dB, hence doubles the line of sight range on raw data
- Customisable to different data, preamble timing requirements (e.g. NMEA sentences)
- Supply Voltage: 3 to 5V
- Small size: 18.5 x 10 x 5.5mm
- Pin outs and foot print compatible with Radiometrix SIL Receivers

Compared to conventional Data Slicer circuit currently used in the most of the FSK receivers, Quasi DC Recovery circuit can extract non-bit balanced data at RF signal level that is 6dB lower, resulting in double the range.

Conventional Data Slicers are based on simple 'RC integrate and compare' method to digitise the demodulated analogue signal, whereas, the QR96 samples positive and negative peaks of the Audio (AF) output and then averages them, before using that voltage as the comparator reference. QR96 behaves better on very unbalanced (raw) data, and at the start of bursts (where the simple RC takes time to acquire or charged to the mid average point).

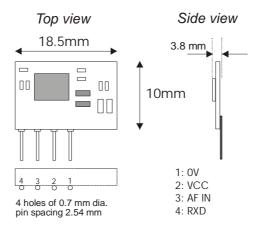


Figure 2: QR96 pin-out and dimension

| QR96 pin | Name | Function |
|----------|-------|---|
| 1 | 0V | DC supply ground |
| 2 | Vcc | 3 – 5V |
| 3 | AF in | AF input is connected to the AF output of the receiver, requires signal level |
| | | of 0.6V – 1.2V peak to peak on top of a DC bias level of 0.5-1.5V. |
| 4 | RXD | Received Data output is open collector, an external $10k\Omega$ pull-up resistor to |
| | | the VCC is required. RXD will be inverted with respect to AF In. |

Note: 20ms of preamble (55hex or square wave signal) should be received from transmitter for the mark:space ratio of the RXD to stabilise to 50:50 on standard QR96. However, data packets with gaps >250ms (e.g. GPS NMEA data) would require extended preamble of up to 100ms.

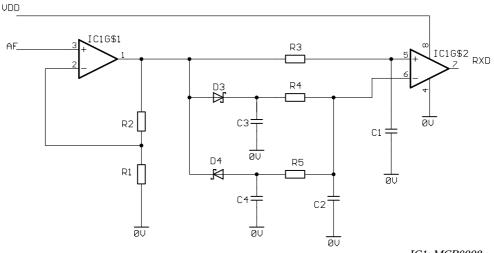


Figure 3: Schematics of QR96



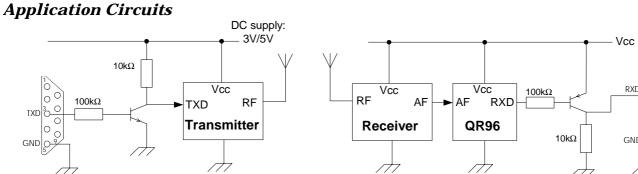


Figure 4: Typical wireless RS232 interface with RF modules and QR96

С