NEW

Radiometrix

Hartcran House, 231 Kenton Lane, Harrow, HA3 8RP, England
Tel: +44 (0) 20 8909 9595, Fax: +44 (0) 20 8909 2233

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TDL3F

Transparent Data Link on 868/914MHz band

A TDL3F is a single channel, 869 or 915MHz wideband, transparent data link. It has a TDL2A pin out (and firmware), but uses a BiM3 series radio module. TLD3F acts as a transparent serial cable to attached host. TDL3F is an intermediate level OEM radio modem which is in between a raw FM radio module like BiM3B and a sophisticated OEM radio modem like RPM3. It takes care of preamble, synchronisation, bit balancing and error checking along with automatic noise squelching.

Figure 1: TDL3F-868.30-9 radio modem

The TDL3F provides a half duplex link. Provided no two devices attempt to transmit simultaneously no further restrictions on data transmission need be made, as all transmit timing, valid data identification and datastream buffering is conducted by the unit. Synchronisation and framing words in the packet prevent the receiver outputting garbage in the absence of wanted RF signal or presence of interference**.** For multiple radio systems (polled networks) a TDL3F can be set to 1 of 8 unique addresses.

Features

- Conforms to EN 300 220-3 and EN 301 489-3
- Crystal controlled PLL FM circuitry for both Tx and Rx
- SAW front-end filter
- Single conversion superhet
- Serial modem baud rate at 9600bps (half-duplex)
- Addressable point-to-point

Applications

- PDAs, organisers & laptops
- Handheld / portable terminals
- EPOS equipment, barcode scanners
- In-building environmental monitoring and control
- Remote data acquisition system, data logging
- Fleet management, vehicle data acquisition

Technical Summary

- Operating frequency: 869.85 / 868.30MHz (Europe), 914.5MHz (North America)
- Modulation: 16kbps bi-phase FSK
- Supply: 5V at 18mA transmit (@5mW), 15mA receive/idle
- Transmit power: +5mW @ 869.85MHz)
- Receiver sensitivity: -106dBm (for 1% BER)
- 32 byte data buffer

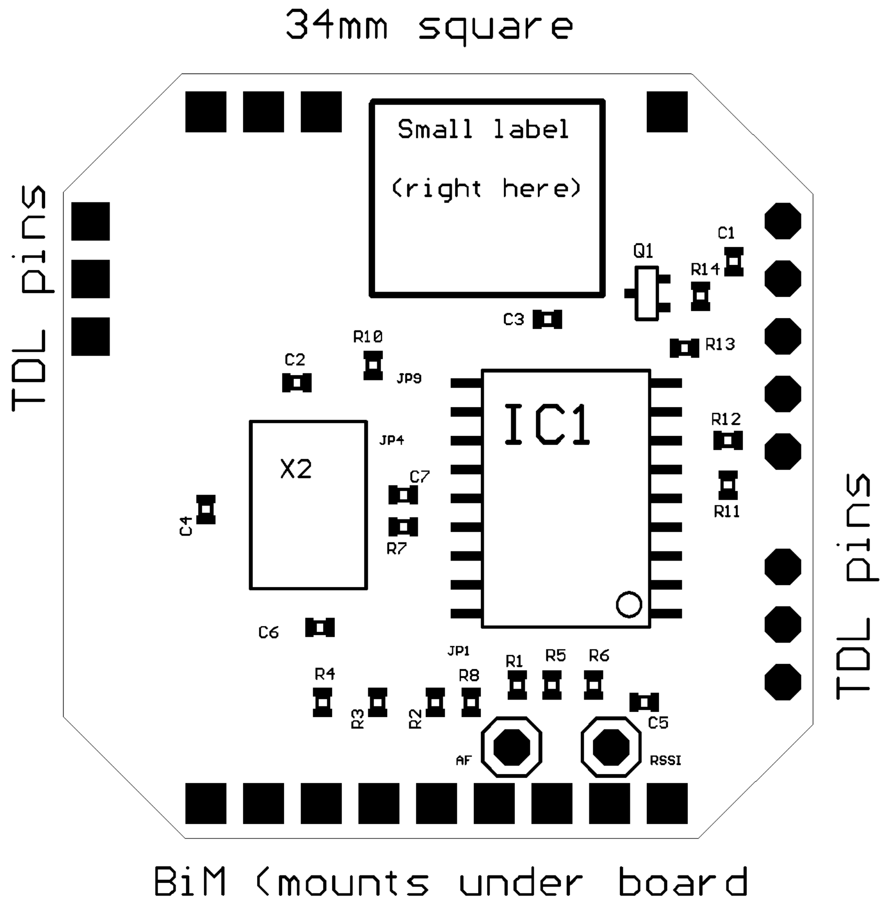

Figure 2: TDL3F footprint (top view)

Pin description

Pin	Name	Function
18	GND	Ground
17	Vcc	5V regulated power supply (4.75 - 5.25v)
16	$\overline{\text{ENABLE}}$	Enable or DTR (5V CMOS logic level input)
15	$\overline{\text{SETUP}}$	Test/Setup mode selection (5V CMOS logic. Pull up to 5V)
14	TXD	Transmit Data (Inverted RS232 at 5V CMOS logic, No pullup)
13	NC	No Pin
12	RXD	Receive Data (Inverted RS232 at 5V CMOS logic output)
11	STATUS	Busy or $\overline{\text{CTS}}$ (5V CMOS logic level output)
10	GND	Ground

NOTE:
1. Pinout is as TDL2A. On RF connector end only pins 1,2,3 are present.
2. TXD / RXD are inverted RS232 at 5v cmos levels. To connect to a true RS232 device, inverting level shifters must be used (MAX232 type are ideal, but simple NPN transistor switches with pullups often suffice). With typical microcontrollers and uarts, direct connection is possible.
2a An interface board which takes a BiM3 series transceiver is offered, called TDi3 . This has MAX232 type buffer, 9 way D connector, 5v voltage regulator, SMA RF connector and all the processor and interface circuitry of the TDL3F. This board is 61mm x 33mm in size.
3. The TDL3F provides a half duplex link, but provided no two devices attempt to transmit at one time (a 'low' on RX_busy may be used as a primitive 'CTS' indication) no further restrictions on data transmission need be made, as all transmit timing, valid data identification and datastream buffering is conducted by the unit. There is no 'transmit enable' pin.
Sync and framing words in the packet prevent the receiver outputting garbage in the absence of signal or presence of interference.
4. A simple addressing structure is included in the datastream. Units may be programmed onto one of eight addresses (all units are supplied set to default addr=0)
5. TDL3F uses a BiM3 series transceiver module (e.g. BiM3A-914-64, BiM3B-869-64)
6. This unit is programmed exactly as a TDL2A, with the channel select commands being ignored.

RF GND *pin 1 & 3*
RF Ground pin, internally connected to the module screen and pin 8, 9, 10 and 18 (0V). This pin should be connected to the RF return path (e.g. co-axial cable braid, main PCB ground plane, etc).

RF *pin 2*
50Ω RF input/output from the antenna, it is DC isolated internally. (see antenna section for details).

GND *pin 8, 9, 10 and 18*
Supply ground connection to ground plane and can.

VCC *pin 17*
5V voltage regulator should be used to have a clean 5V supply to the module

$\overline{\text{ENABLE}}$ *pin 16*
Active low Enable pin. It has a 10kΩ pull-ups to Vcc. It should be pulled Low to enable the module. This can also be connected to DTR pin (only if it is asserted by the host) of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter.

$\overline{\text{SETUP}}$ *pin 15*
Active low input to enter configuration or diagnostic test mode. It has a 10kΩ pull-ups to Vcc

TXD *pin 14*
This is inverted RS232 data input at 5V CMOS logic level. It can be directly interfaced to data output of a UART in a microcontroller or to a TXD pin of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter. TXD does not have an internal pull-up. If TDL3F is used in Receive only mode, TXD should be tied to Vcc.

NC *pin 13*
There is no pin in this position.

RXD *pin 12*
This is inverted RS232 data output at 5V CMOS logic level. It can be directly interfaced to data input of a UART in a microcontroller or to a RXD pin of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter.

STATUS *pin 11*
This pin goes high when valid data is present in the receive buffer. It can be used to trigger an interrupt in the host to download received data packet instead of waiting for it. It can be also be used as a primitive CTS signal. It is inverted RS232 data output at 5V CMOS logic level. It can be directly interfaced to an input of a microcontroller as a Data Detect (DD) or to CTS, DSR, DCD pins of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter. This is can only be used to prevent host from uploading any data before downloading already received data, because transmission is prioritised over reception and any data to be transmitted will erase received data which is in the common buffer.

Serial interface – modem operation

To connect to a true RS232 device, inverting RS232-CMOS level shifters must be used. Maxim MAX232 or equivalent are ideal, but simple NPN transistor switches with pull-ups often suffice. With typical microcontrollers and UARTs, direct connection is possible.

The Radio / data stream interface

A 32 byte software FIFO is implemented in both the transmit and receive sub-routine. At the transmitting end this is used to allow for the transmitter start up time (about 4mS), while on receiving end it buffers arriving packets to the constant output data rate. All timing and data formatting tasks are handled by the internal firmware. The user need not worry about keying the transmitter before sending data as the link is entirely transparent.

For transmission across the radio link data is formatted into packets, each comprising 3 bytes of data and a sync code. If less than 3 bytes are in the transmit end FIFO then a packet is still sent, but idle codes replaces the unused bytes. When the transmit end FIFO is completely emptied, then the transmitter is keyed off.

Operation: Radio interface.

Raw data is not fed to the radios. A coding operation in the transmit sub-routine, and decoding in the receiver, isolate the AC coupled, potentially noisy baseband radio environment from the datastream.

The radio link is fed a continuous tone by the modem. As in bi-phase codes, information is coded by varying the duration consecutive half-cycles of this tone. In our case half cycles of 62.5us and 31.25us are used. In idle (or 'preamble') state, a sequence of the longer cycles is sent (resembling an 8KHz tone).

A packet comprises the Synchronising (or address) part, followed by the Data part, made up of twelve Groups (of four half cycles duration). Each Group encodes 2 data bits, so one byte is encoded by 4 Groups.

Programming the TDL3F

In order to use all the functions embedded in the TDL3F, the user must be aware of the setup/programming facility, which allow different addresses and frequency channels to be set up, and if necessary accesses diagnostic test modes.

The TDL3F is programmed through the same RS232 port that is used for sending/receiving data. An RS232 terminal emulator (such as Aterm or HyperTerminal) is an ideal tool.

To enter program mode, the **SETUP pin** must be **pulled low**. In this mode the radio link is disabled, but characters sent (at 9600 baud, as normal) to the unit are echoed back on the RXD pin.

The unit will only respond to certain command strings:

ADDR0 to **ADDR7** <CR>: These commands set up one of 8 unique addresses.

A TDL3F will only communicate with a unit set to the same address.

Address and channel numbers are stored in volatile memory. On power-up the TDL3F reverts to the default in EEPROM (as supplied this is always address 0)

SETPROGRAM <CR>: Writes the current address and current channel into EEPROM as the new default.
A tilda character (~, ascii 126dec) sent by the unit indicates end of EEPROM write sequence

(these commands are normally only used for factory diagnostics)
NOTONE <CR>: Transmit unmodulated carrier
LFTONE <CR>: Transmit carrier modulated with 8KHz squarewave
HFTONE <CR>: Transmit carrier modulated with 16KHz squarewave
<CR>: Transmitter off

A Carriage Return ‘<CR>’ (00Dhex) should be entered after each command sequence to execute it.

Releasing the SETUP pin to high state returns the TDL3F to normal operation.

Interfacing a microcontroller to TDL3F

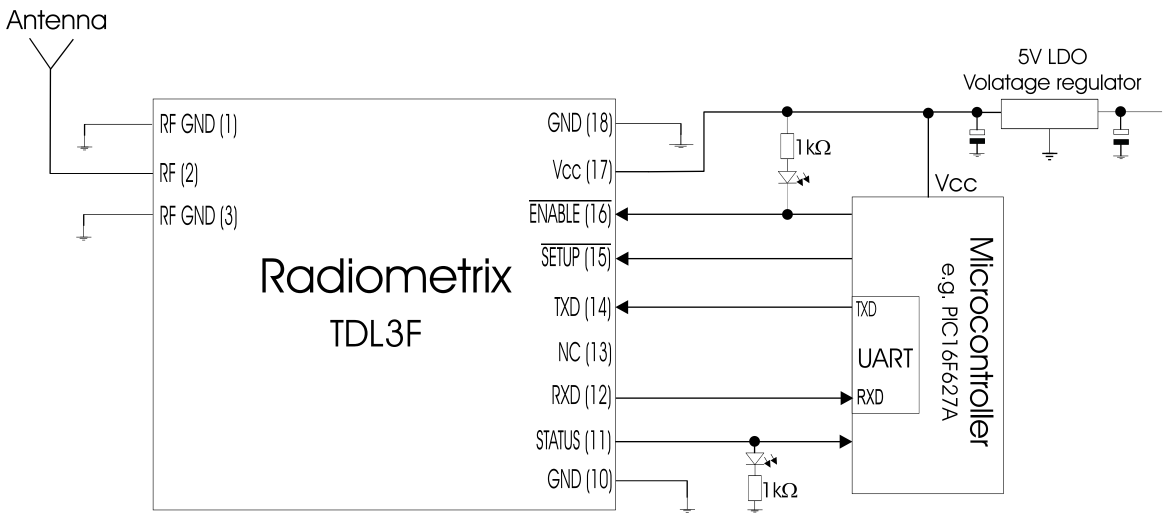

Figure 5: TDL3F interfaced directly to a microcontroller

TDL3F can be directly interfaced to any microcontrollers. If the microcontroller has a built-in UART, it can concentrate on its main task and leave the packet formatting, bit balancing and error checking of serial data to TDL3F.

Serial data should be in the following format:

1 start bit, 8 data bits, no parity, 1 or 2 stop bits
9600bps
0V=low, 5V=high

STATUS pin can be connected to one of the port pins which can generate an interrupt on low-to-high transition (e.g. RB0/INT pin in the PIC). This can be used to enter a receive sub-routine to download data received from remote TDL3F. Therefore, the host does not need to wait in a loop for a packet.

Range test and site survey can be carried out by connecting an LED on the STATUS pin. Every time, TDL3F is within range to receive valid data, the LED will flicker.

Interfacing TDL3F to an RS232 port

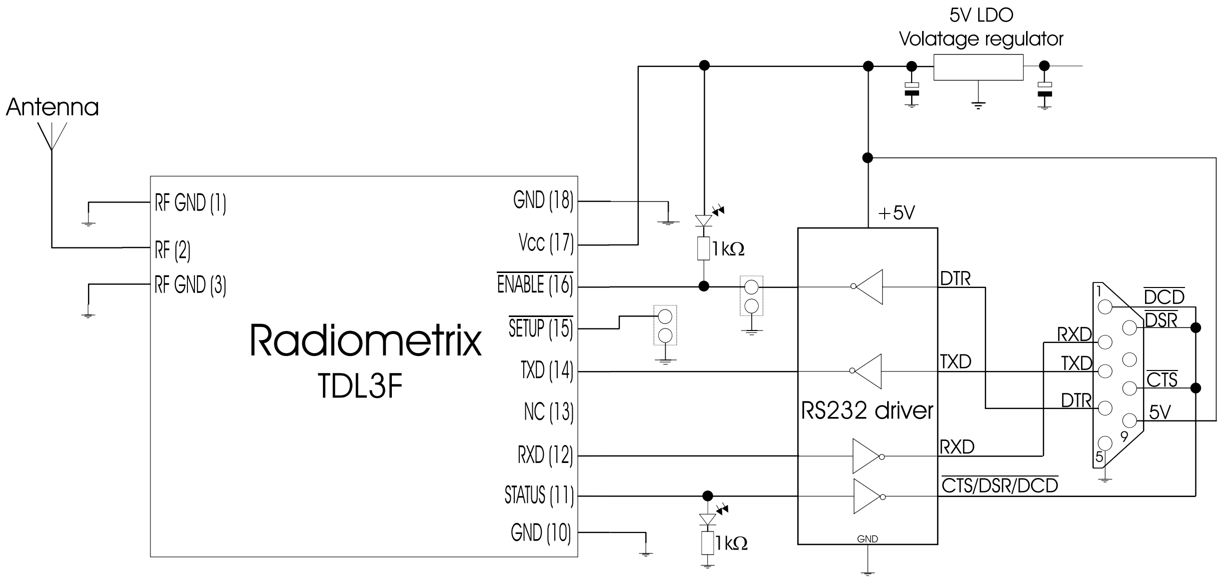

Figure 6: TDL3F interfaced to an RS232 port via an RS232 line driver/receiver

STATUS pin in this can be connected to CTS, DSR and DCD pin to simulate a flow control signal.

TDL3F is capable of continuously streaming data at 9600bps. Therefore, STATUS pin is not asserted to stop the Host from sending data as in normal RTS/CTS flow control method, but merely to warn the host that there is already data in the receive buffer which need to be downloaded before sending any more data.

Some DTE hosts assert DTR signal when they are active and this can be used via RS232 line receiver to enable TDL3F. Otherwise the ENABLE must be physically pulled-low to activate the TDL3F.

NOTE:
An interface board (with MAX232 type buffer, 9 way D connector, 5V voltage regulator and SMA RF connector) is available. This board is 61mm x 33mm in size.

Condensed specifications

Frequency	868.30MHz or 869.85MHz (Europe) 914.5MHz (North America)
Frequency stability	±25kHz
Channel width	400kHz
Number of channels	1
Supply *Voltage*	5V
Current Transmit	40mA @ 868.30MHz, 18mA @ 869.85MHz, 12mA @ 914.5MHz
Receive/idle	15mA
Operating temperature	-20 °C to +70 °C (Storage -30 °C to +70 °C)
Spurious radiations	Compliant with ETSI EN 300 220-3 and EN 301 489-3
Interfaces	
User	9pin 0.1" pitch molex (pin 6 absent)
RF	3pin 0.1" pitch molex
Size	34 x 33 x 10mm

Transmitter	
Output power	25mW @ 868.30MHz 5mW @ 869.85MHz -1dBm (0.75mW) @ 914.5MHz
Duty cycle limit	1% @ 868.30MHz 100% @ 869.85MHz 100% @ 914.5MHz
TX on switching time	<4ms
Modulation type	16kbps bi-phase FSK
FM peak deviation	+/-40KHz (typ.)
TX spurious	<-40dBm
Receiver	
Sensitivity	-106dBm for 1% BER
spurious / adjacent channel	-50dB
LO re-radiation	<-100dBm typ.
Interface	
Data rate	9600baud, Half duplex
Format	1 start, 8 data, 1 stop, no parity
Levels	5V CMOS (inverted RS232. Mark = 5V = idle)
Buffers	32 byte FIFO
Flow control	None ('RX busy' pin provided)
Addressing	1 of 8, user programmed
Data latency	14ms (first byte into TX, to first byte out of RX)

Antenna considerations and options

The choice and positioning of transmitter and receiver antennas is of the utmost importance and is the single most significant factor in determining system range. The following notes are intended to assist the user in choosing the most effective arrangement for a given application.

Nearby conducting objects such as a PCB or battery can cause detuning or screening of the antenna which severely reduces efficiency. Ideally the antenna should stick out from the top of the product and be entirely in the clear, however this is often not desirable for practical or ergonomic reasons and a compromise may need to be reached. If an internal antenna must be used, try to keep it away from other metal components and pay particular attention to the “hot” end (i.e. the far end), as this is generally the most susceptible to detuning. The space around the antenna is as important as the antenna itself.

Microprocessors and microcontrollers tend to radiate significant amounts of radio frequency hash, which can cause desensitisation of the receiver if its antenna is in close proximity. 915MHz is generally less prone to this effect than lower frequencies, but problems can still arise. Things become worse as logic speeds increase, because fast logic edges are capable of generating harmonics across the UHF range which are then radiated effectively by the PCB tracking. In extreme cases system range can be reduced by a factor of 3 or more. To minimise any adverse effects, situate the antenna and module as far as possible from any such circuitry and keep PCB track lengths to the minimum possible. A ground plane can be highly effective in cutting radiated interference and its use is strongly recommended.

Two types of antenna are recommended for use with the TDL3F:

Whip (¼-wave): This consists simply of a piece of wire or rod connected to the module at one end. The lengths given below are from module pin to antenna tip including any interconnecting wire or tracking (but NOT including any 50µ coax or microstrip connection). This antenna is simple, cheap, easy to set up and performs well. It is especially effective when used with a ground plane, which in practice is often provided by the main PCB or by a metal case.

Base-loaded whip: In applications where space is at a premium a shortened whip may be used, tuned by means of a coil inserted at the base. This coil may be air-wound for maximum efficiency, or a small SMT inductor can be used. The value must be empirically chosen to tune the particular length of whip for best results “in situ”, making this antenna more difficult to set up. Radiated power will generally be slightly less than that obtained from a ¼-wave whip.

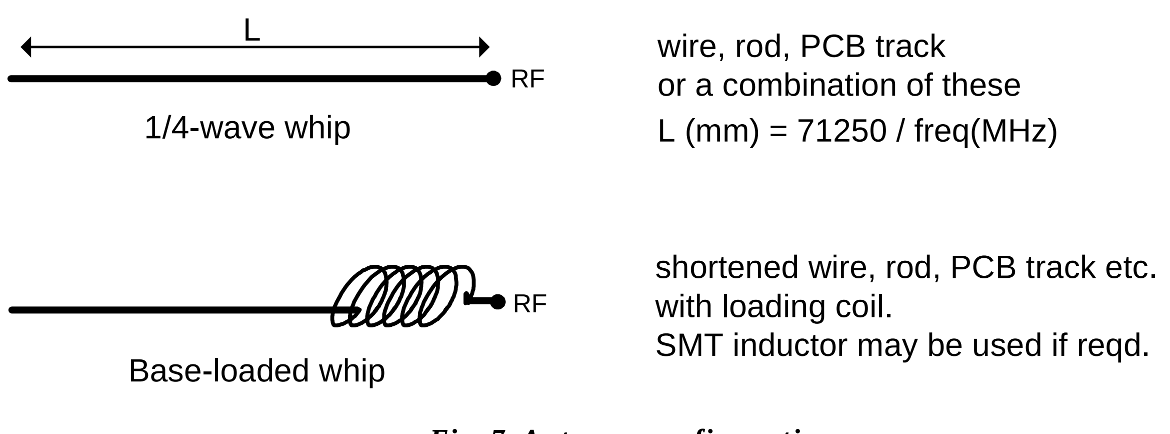

Fig. 7: Antenna configurations

Other types of antennas are feasible but tend to have drawbacks at these frequencies. Helical and tuned loop antennas are both very compact but tricky to set up, and can be impractical at 915MHz because of their very small size. Microstrip patch antennas are relatively large in area, directional, and have gain. These characteristics can be useful but tend to preclude FCC Part 15.249 applications, as it is easily possible to exceed the limit for radiated field strength.

Note: Where the specified antennas are mounted on the PCB and/or in close proximity to metalwork (module casing, components, PCB tracking etc), the antenna radiation pattern may be seriously affected. Radiated power may be significantly increased in some directions (sometimes by as much as 10dB) and correspondingly reduced in others. This may adversely affect system performance where good all-round coverage is desired.

Care should also be taken to ensure that this effect does not increase the radiated power in any direction beyond that allowed by type approval regulations. Where this occurs the antenna may need to be relocated. In extreme cases a resistive attenuator of appropriate value may be required between the module and antenna.

Ordering information

The TDL3F radio modem is manufactured in the following variants as standard:

Part Number	Frequency band	RF power (typ.)	Baud rate
TDL3F-869.85-9	869.85 MHz	5mW	9.6kbps
TDL3F-868.30-9	868.30 MHz	25mW	9.6kbps
TDL3F-914.50-9	914.50 MHz	1mW	9.6kbps

Radiometrix Ltd

Hartcran House
231 Kenton Lane
Harrow, Middlesex
HA3 8RP
ENGLAND
Tel: +44 (0) 20 8909 9595
Fax: +44 (0) 20 8909 2233
sales@radiometrix.com
www.radiometrix.com

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The Intrastat commodity code for all our modules is: 8542 6000.

R&TTE Directive

After 7 April 2001 the manufacturer can only place finished product on the market under the provisions of the R&TTE Directive. Equipment within the scope of the R&TTE Directive may demonstrate compliance to the essential requirements specified in Article 3 of the Directive, as appropriate to the particular equipment.
Further details are available on The Office of Communications (Ofcom) web site:
http://www.ofcom.org.uk/radiocomms/ifi/

Information Requests
Ofcom
Riverside House
2a Southwark Bridge Road
London SE1 9HA
Tel: +44 (0)845 456 3000 or 020 7981 3040
Fax: +44 (0)20 7783 4033
information.requests@ofcom.org.uk

European Radiocommunications Office (ERO)
Peblingehus
Nansensgade 19
DK 1366 Copenhagen
Tel. +45 33896300
Fax +45 33896330
ero@ero.dk
www.ero.dk